WT61P8
Flat Panel Display Control Sub-MCU

Data Sheet

Rev. 1.01

April 17, 2008

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REVISION HISTORY

V1.01 04/17/2008 This Book
1. Add CEC application circuit on section 7.4
2. Update Electrical characteristics description

V1.00 11/26/2007

V0.98 7/16/2007
3. Update DDC/IIC data flow and flow chart on page 34~39.
4. Update electrical characteristic.

V0.97 7/3/2007
5. Update DDC/IIC register description, data flow and flow chart on page 34~39.
6. Add product Tube and Tape & Reel specifications
7. Update "MCU clock option diagram" on page 14

V0.96 6/7/2007
8. Add HV sync process block diagram on page 24.
9. Update PWM_CLK description on system level register.
10. Change Flash memory size to 64K from 52K
11. Update SFR register description on page 10~12
12. Update All register map on page41~42

V0.95 5/07/2007
1. Add XTAL_CLK(index 01H-bit2) for XTAL clock divider.
2. Update PWM_CLK description on system level register.
3. Add "WDT[2]" (index08-bit2) for watchdog timer reset pulse selector.
4. Change flash memory size to 52k from 64k.

V0.94 4/4/2007
1. Update UART naming
2. Add RTC block diagram in chapter 4.14
3. Update system reset description.

V0.93 2/8/2007
1. Update T2CON register on page 12.
2. Add interrupt flow chart on page 20.

V0.92 2/5/2007
1. Update memory mapping on page 8.

V0.91 1/30/2007
1. Update function block diagram on page 7.
2. Update HV Sync DPMS detector diagram on page 22.

V0.90 1/27/2006
Preliminary data sheet.

Table of Contents

1 General Description

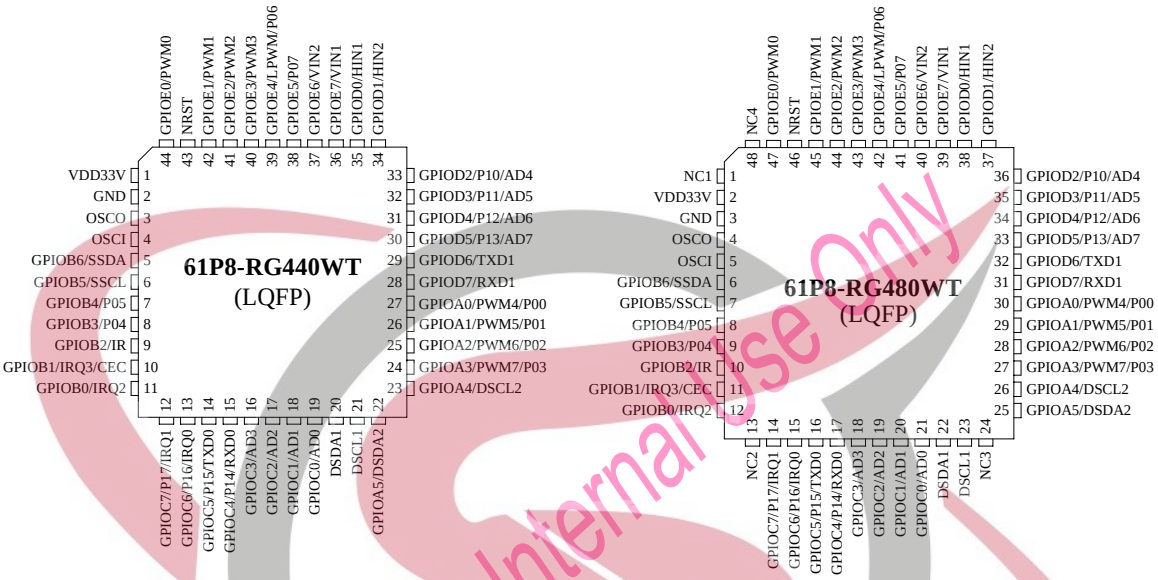
The WT61P8 is a microcontroller for flat panel display control and power management with 1) Turbo 8052 CPU, 2) 64K bytes flash memory, 3) 1K+256 bytes SRAM, 4) 8 8-bit PWMs, 5) DPMS detector(2 H/V inputs, Support H+V input) , 6) 4 timers and 2 UART Ports, 7) 2 DDC/CI interface, 8) Slave I2C interface, 9) 8 channel 8-bit A/D converter, 10) Real Time Clock, 11) Watch-dog timer, 12) Embedded ISP function, 13) Power down mode, 14) Embedded ICE mode. 15) H/W CEC

1.1. Features

- Embedded Turbo 8052 CPU
  - Normal operation mode: 12MHz, 6MHz, 3MHz, 1MHz or 24MHz, 12MHz, 6MHz, 2MHz (Selectable Clock Sources)
  - Instruction execution time : Min. =250ns at OSC=12Mhz
- Memory:
  - RAM: 1K+256 Bytes
  - Flash memory : 64K Bytes
- 4 similar 8052 timers: Timer0, Timer1, Timer2, Timer3
- 2 similar 8052 UART ports, support baud rate 115200 – 1200 at OSC = 12MHz
- Sync processor for monitoring DPMS (support 2 H/V inputs, Support H+V inputs) wake up signal.
- 8-bit A/D converter with 8 selectable inputs, shared with IO pin
- 8 8-bit PWM pin output (One low frequency PWM at 150Hz for dimmer control)
- Support 2 DDC/CI interface
- Slave mode I2C interface
- Maximum 37 programmable IO pins
- Hardware universal IR Receiver
- Watch Dog timer
- Build-in RTC
- Build-in ISP function
- Embedded ICE mode
- Embedded H/W CEC function
- Power down mode
  - Selectable CPU clock sources
  - CPU off mode can be waked up by external interrupt
- Operating temperature : -10 to +85 degree C

2. Pin Assignment

2.1. Package



2.2. Ordering information

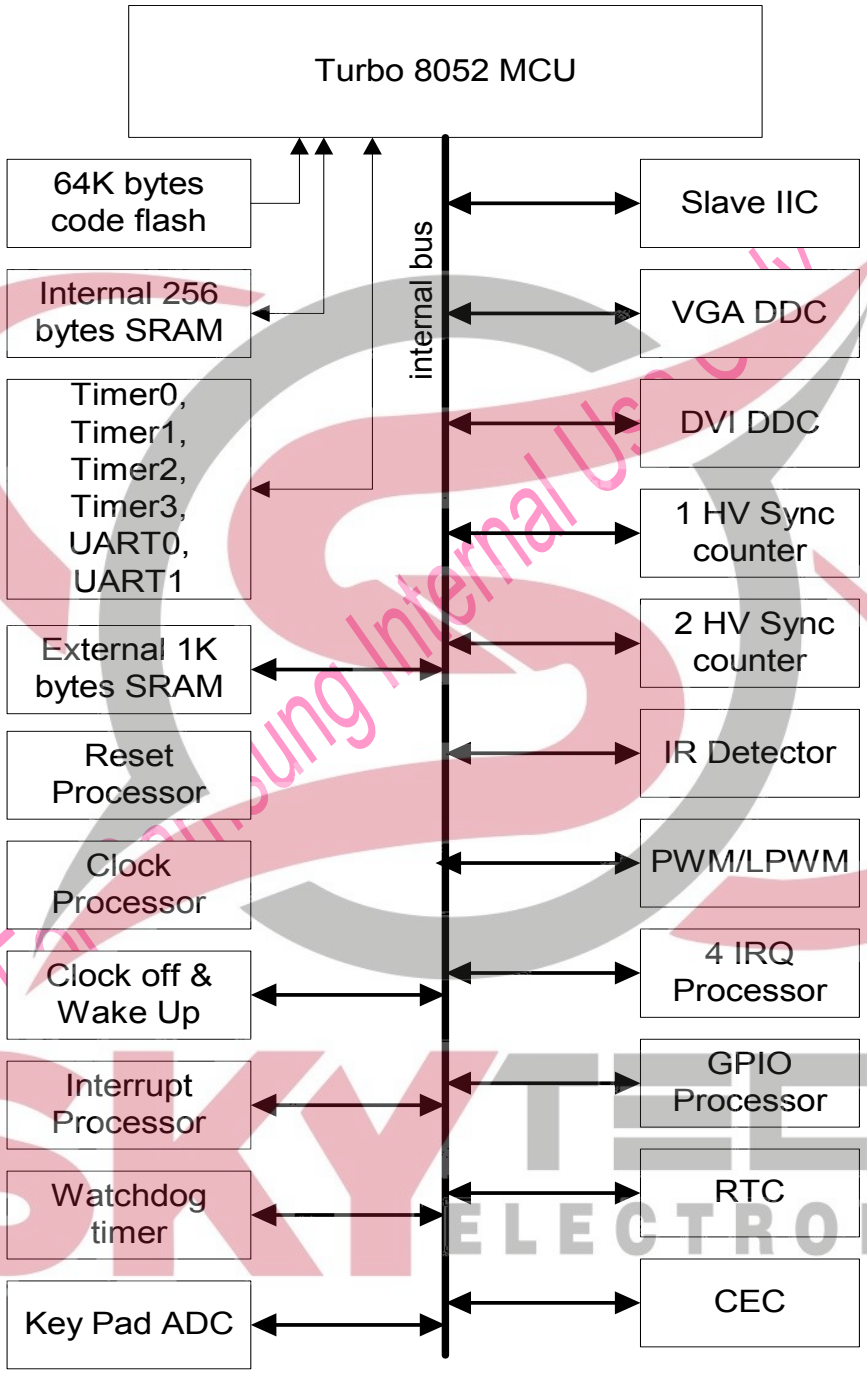
Package Type	Part Number
44-pin LQFP(10x10mm)	61P8-RG440WT
48-pin LQFP(7x7mm)	61P8-RG480WT

2.3. Pin description

RG440	RG480	Pin Name	I/O	Function Description
39	42	GPIOE4	I/O	GPIO E4 share with Low frequency PWM output or 8052 P0.6.
40	43	GPIOE3	I/O	GPIO E3 share with PWM3 output.
41	44	GPIOE2	I/O	GPIO E2 share with PWM2 output.
42	45	GPIOE1	I/O	GPIO E1 share with PWM1 output.
43	46	NRST	I/O	Reset pin, active low (internal pull high)
44	47	GPIOE0	I/O	GPIO E0 share with PWM0 output.
1	2	VDD	PWR	Power 3.3V
2	3	VSS	PWR	Ground
3	4	OSCO	OSC	12Mhz(or 24MHz) oscillator output
4	5	OSCI	OSC	12Mhz(or 24MHz) oscillator input
5	6	GPIOB6	I/O	GPIO B6 share with slave IIC SDA.
6	7	GPIOB5	I/O	GPIO B5 share with slave IIC SC L.
7	8	GPIOB4	I/O	GPIO B4 share with 8052 P0.5.
8	9	GPIOB3	I/O	GPIO B3 share with 8052 P0.4.
9	10	GPIOB2	I/O	GPIO B2 share with IR detector input.
10	11	GPIOB1	I/O	GPIO B1 share with HDMI CEC input or external IRQ3 interrupt input.
11	12	GPIOB0	I/O	GPIO B0 share with External IRQ2 interrupt input.
12	14	GPIOC7	I/O	GPIO C7 share with External IRQ1 interrupt input or 8052 P1.7.
13	15	GPIOC6	I/O	GPIO C6 share with External IRQ0 interrupt input or 8052 P1.6.
14	16	GPIOC5	I/O	GPIO C5 share with 8052 UART0 TXD or 8052 P1.5.
15	17	GPIOC4	I/O	GPIO C4 share with 8052 UART0 RXD or 8052 P1.4.
16	18	GPIOC3	I/O	GPIO C3 share with ADC input3.
17	19	GPIOC2	I/O	GPIO C2 share with ADC input2.
18	20	GPIOC1	I/O	GPIO C1 share with ADC input1.
19	21	GPIOC0	I/O	GPIO C0 share with ADC input0.
20	22	DSDA1	I/O	1st DDC SDA1.
21	23	DSCL1	I/O	1st DDC SCL1.
22	25	GPIOA5	I/O	GPIO A5 share with 2nd DDC SDA2.
23	26	GPIOA4	I/O	GPIO A4 share with 2nd DDC SCL2.
24	27	GPIOA3	I/O	GPIO A3 share with PWM7 output or 8052 P0.3.
25	28	GPIOA2	I/O	GPIO A2 share with PWM6 output or 8052 P0.2.
26	29	GPIOA1	I/O	GPIO A1 share with PWM5 output or 8052 P0.1.
27	30	GPIOA0	I/O	GPIO A0 share with PWM4 output or 8052 P0.0.
28	31	GPIOD7	I/O	GPIO D7 share with 8052 UART1 RXD.
29	32	GPIOD6	I/O	GPIO D6 share with 8052 UART1 TXD.
30	33	GPIOD5	I/O	GPIO D5 share with ADC input7 or 8052 P1.3.
31	34	GPIOD4	I/O	GPIO D4 share with ADC input6 or 8052 P1.2.
32	35	GPIOD3	I/O	GPIO D3 share with ADC input5 or 8052 P1.1.
33	36	GPIOD2	I/O	GPIO D2 share with ADC input4 or 8052 P1.0.
34	37	GPIOD1	I/O	GPIO D1 share with 2nd HIN input.
35	38	GPIOD0	I/O	GPIO D0 share with 1st HIN input.
36	39	GPIOE7	I/O	GPIO E7 share with 1st VIN input.
37	40	GPIOE6	I/O	GPIO E6 share with 2nd VIN input.
38	41	GPIOE5	I/O	GPIO E5 share with 8052 P0.7.

(a) All GPIOs have Schmitt trigger input.
(b) When use slave I2C or DDC or 8052 P1.or UART or CEC, the external circuit need pull high
(c)GPIOC3,GPIOC2,GPIOC1,GPIOC0,GPIOD2,GPIOD3,GPIOD4,GPIOD5 MAX input are +3.6v (=3.3v+0.3v) and the other GPIOs MAX input is +5.5v (=5.0v+0.5v)

3. Functional Block Diagram



4. Functional Description

4.1. MCU

4.1.1. Internal MCU

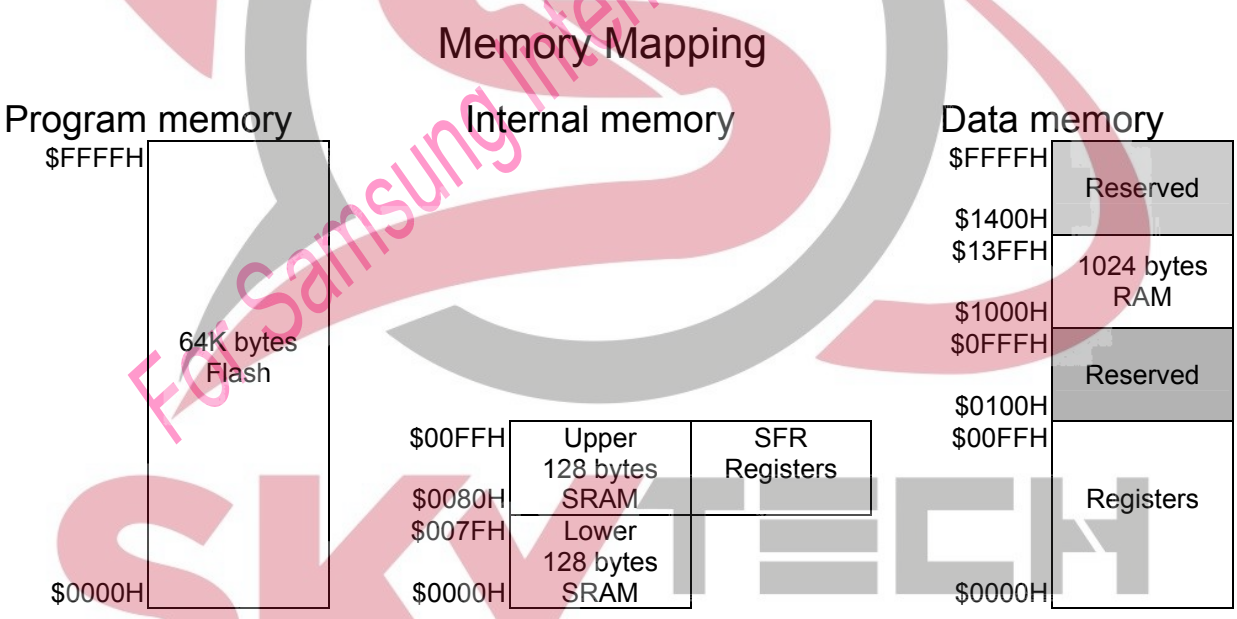
Embedded 8-bit turbo 8052 compatible CPU with 16-bit address and 8-bit data bus operates at 12MHz,6MHz,3Mhz,1Mhz or 24MHz, 12MHz, 6MHz, 2MHz

4.1.2. RAM

The SRAM include :
128 bytes internal SRAM are from 0x0000H to 0x007FH (direct & indirect addressing)
128 bytes internal SRAM are from 0x0080H to 0x00FFH (indirect addressing)
1K bytes external SRAM are from 0x1000H to 0x13FFH

4.1.3. Flash Memory

MAX F/W program address is located from $0000H to $FFFFH (64k bytes).



4.1.4. 8052 Timer0,Timer1,Timer2,Timer3,UART0,UART1,INT1,INT2,INT3

INT1/INT2 is cause by 1st DDC,2nd DDC,HV DPMS detector, IR detector, CEC detector, Key pad ADC, input toggle interruption.
INT3 is cause by slave IIC
If UART0 is used, the EN_UART0_IO register has to be set "1".
If UART1 is used, the EN_UART1_IO register has to be set "1".

4.1.5. SFR(SPECIAL FUNCTION REGISTER) MAP

F8								FF
F0	B							F7
E8	T3CON		RCAP3L	RCAP3H	TL3	TH3		EF
E0	ACC							E7
D8	SCON1	SBUF1	SBRG1					DF
D0	PSW							D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2		CF
C0	XICON							C7
B8	IP	IP2						BF
B0	*P3*							B7
A8	IE	IE2						AF
A0	*P2*							A7
98	SCON	SBUF	SBRG0					9F
90	*P1*							97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKSEL	8F
80	*P0*	SP	DPL	DPH			PCON	87

☝ bit addressable

Nine-source interrupt information:

Interrupt Source	Vector Address	Polling Sequence within Priority level	Enabled required settings	Interrupt type edge/level
Timer/Counter 0	0BH	1	IE.1	--
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	--
Serial Port 0 (UART0)	23H	4	IE.4	--
Timer/Counter 2	2BH	5	IE.5	--
Serial Port 1 (UART1)	33H	6	IE.6	--
External Interrupt 2	3BH	7	XICON.2	XICON.0
External Interrupt 3	43H	8	XICON.6	XICON.4
Timer/Counter 3	4BH	9(lowest)	IE2.0	--

XICON (8052 interrupt enable and priority register) Address : C0H

Index	Default	R/W	Bit	Name	Description
C0	00	R/W	7	PX3	External interrupt 3 priority high if set

			6	EX3	External interrupt 3 enable if set
			5	IE3	If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced
			4	IT3	External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software
			3	PX2	External interrupt 2 priority high if set
			2	EX2	External interrupt 2 enable if set
			1	IE2	If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced
			0	IT2	External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

The XICON register is bit-addressable but is not a standard register in the standard 8052. Its address is at C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB C2H" sets the EX2 bit of XICON.

IE (8052 interrupt enable register) Address : A8H

7	6	5	4	3	2	1	0
EA	ES1	ET2	ES	ET1	EX1	ET0	EX0

ES1 :IE.6, Enables/disables the Serial Port 1 interrupt. If ES1 = 0, the Serial Port 1 interrupt is disabled.

IE2 (8052 interrupt enable register2) Address : A9h

7	6	5	4	3	2	1	0
							ET3

ET3:IE2.0, Enables or disables the Timer 3 interrupt. If ET3=0, the Timer 3 interrupt is disabled.

IP (8052 interrupt priority register) Address : B8H

7	6	5	4	3	2	1	0
	PS1	PT2	PS	PT1	PX1	PT0	PX0

"PS1" : IP.6, Define the serial port 1 interrupt priority level. PS1 = 1 program it to higher priority level.

IP2 (8052 interrupt priority register2) Address : B9h

7	6	5	4	3	2	1	0
							PT3

"PT3": IP2.0, Define the Timer 3 interrupt priority level. PT3 = 1 program it to higher priority level.

SCON1 (8052 UART1 control register) Address : D8H

7	6	5	4	3	2	1	0
SM0_1	SM0_2	SM0_3	REN_1	TB8_1	RB8_1	TI_1	RI_1

The additional serial port is similar as 8052's UART.

SBUF1 (8052 UART1 buffer) Address : D9H

7	6	5	4	3	2	1	0
SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

PCON (8052 power control register) Address : 87H

7	6	5	4	3	2	1	0
SMOD1	SMOD2			GF1	GF0	PD	IDL

SBRG0 (8052 UART0 baud rate control register) Address : 9AH

7	6	5	4	3	2	1	0
SBRG0EN	SBRG0.6	SBRG0.5	SBRG0.4	SBRG0.3	SBRG0.2	SBRG0.1	SBRG0.0

SBRG1 (8052 UART1 baud rate control register) Address : DAH

7	6	5	4	3	2	1	0
SBRG1EN	SBRG1.6	SBRG1.5	SBRG1.4	SBRG1.3	SBRG1.2	SBRG1.1	SBRG1.0

Baud Rate Generation for UART0

SBRG0EN(SBRG0.7)	SMOD1(PCON.7)	SMOD2(PCON.6)	TCS1(CKSEL.2)	Baud Rate for UART0
0	0	0	0	$\frac{1}{32}\times\frac{f_{osc}}{12\times(256-TH1)}$
			1	$\frac{1}{32}\times\frac{f_{osc}}{3\times(256-TH1)}$
0	SMOD1 or SMOD2 = 1		0	$\frac{1}{16}\times\frac{f_{osc}}{12\times(256-TH1)}$
			1	$\frac{1}{16}\times\frac{f_{osc}}{3\times(256-TH1)}$
0	1	1	0	$\frac{1}{8}\times\frac{f_{osc}}{12\times(256-TH1)}$
			1	$\frac{1}{8}\times\frac{f_{osc}}{3\times(256-TH1)}$
1	0	0	X	$\frac{1}{32}\times\frac{f_{osc}}{(SBRG0[6:0]+1)}$
1	SMOD1 or SMOD2 = 1		X	$\frac{1}{16}\times\frac{f_{osc}}{(SBRG0[6:0]+1)}$
1	1	1	X	$\frac{1}{8}\times\frac{f_{osc}}{(SBRG0[6:0]+1)}$

Baud Rate Generation for UART1

SBRG1EN(SBRG1.7)	SMOD2(PCON.6)	TCS2(CKSEL.3)	Baud Rate for UART1
0	0	0	$\frac{1}{16}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
		1	$\frac{1}{16}\times\frac{f_{osc}}{3\times(65536-RCAP2)}$
0	1	0	$\frac{1}{8}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
		1	$\frac{1}{8}\times\frac{f_{osc}}{3\times(65536-RCAP2)}$
1	0	X	$\frac{1}{16}\times\frac{f_{osc}}{(SBRG1[6:0]+1)}$
1	1	X	$\frac{1}{8}\times\frac{f_{osc}}{(SBRG1[6:0]+1)}$

T2CON (8052 Timer 2 control register) Address: C8H

7	6	5	4	3	2	1	0
TF2					TR2		

TF2: Timer 2 Overflow. This bit is set when Timer2 overflows. When Timer2 interrupt is enabled, this bit will cause the interrupt to be triggered.
TR2: Timer 2 Run. When set, timer 2 will be turned on. Otherwise, it is turned off.

T3CON (8052 Timer 3 control register) Address : E8h

7	6	5	4	3	2	1	0
TF3					TR3		

TF3: Timer 3 Overflow. This bit is set when Timer3 overflows. When Timer3 interrupt is enabled, this bit will cause the interrupt to be triggered.
TR3: Timer 3 Run. When set, timer 3 will be turned on. Otherwise, it is turned off.

CKSEL (8052 auxiliary register) Address : 8EH

7	6	5	4	3	2	1	0
				TCS3	TCS2	TCS1	TCS0

TCSx is timer clock-base select bits.

TCSx	Timer clock-base
0	12 clock cycles (Default)
1	3 clock cycles

4.2. System Reset

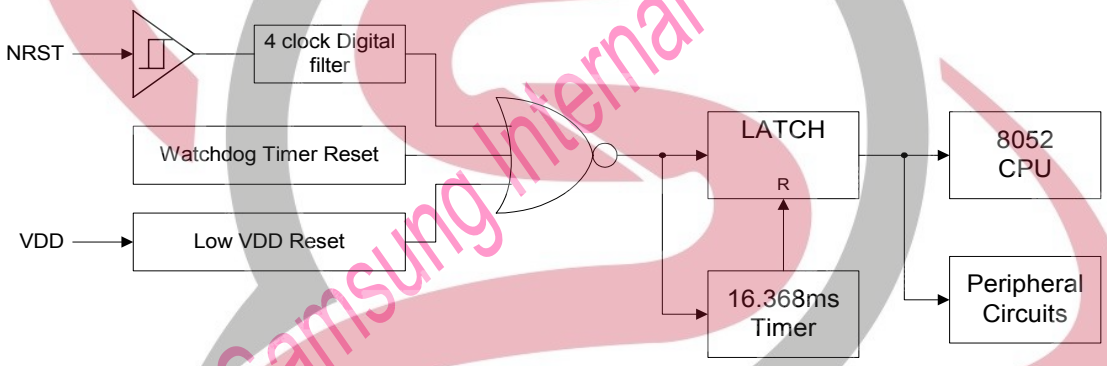
All reset signals will last 16*12*1024*(OSC clock), For waiting system stable

OSC clock = 12MHz, all reset signals will last 16*12*1024*F_{OSC} = 16.384ms
OSC clock = 24MHz, all reset signals will last 16*12*1024*F_{OSC} = 8.192ms

Reset sources
NRST
The NRST-Reset happens when there is a low level on the NRST pin.

Low VDD Reset
The Low-VDD-Reset is generated when VDD is below 2.7v.

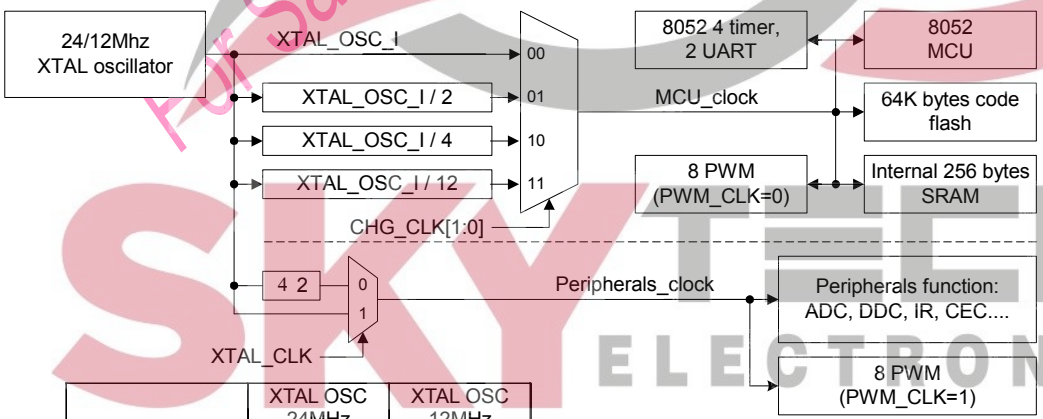
Watchdog Timer Reset
The Watchdog-Timer-Reset happens when the watchdog timer is time out. Please refer to the watchdog timer section for more detail.



4.3. System Level Register

Index	Default	R/W	Bit	Name	Description
01	84	R/W	7	RST_NDF	1: Disable “NRST pin” digital filter(default) 0: “NRST” have digital filter
			6	OSC_OFF	1: Power down mode, turn off all clock & system clock (system no clock) 0: Normal mode.
			5	MCU_OFF	1: Turn off MCU clock, only RTC works 0: MCU ON.
			4	PWM_CLK	PWM clock base, 0: PWM clock base = MCU clock 1: PWM clock base = 1Mhz
			3	Reserved	
			2	XTAL_CLK	XTAL clock divider (Note 1), 1: Peripherals clock is same as XTAL_OSC_I (default) 0: Peripherals clock is XTAL_OSC_I / 2
			1-0	CHG_CLK[1:0]	If XTAL clock is 24MHz and XTAL_CLK=0 00 : MCU clock=24Mhz 01 : MCU clock=12Mhz 10 : MCU clock=6Mhz 11 : MCU clock=2Mhz If XTAL clock is 12MHz and XTAL_CLK=1, 00 : MCU clock=12Mhz 01 : MCU clock=6Mhz 10 : MCU clock=3Mhz 11 : MCU clock=1Mhz

MCU clock option:



	XTAL OSC 24MHz		XTAL OSC 12MHz	
CHG_CLK	00		00	
XTAL_CLK	0	1	0	1
MCU clock	24MHz	24MHz	12MHz	12MHz
Peripherals clock	12MHz	24MHz	6MHz	12MHz

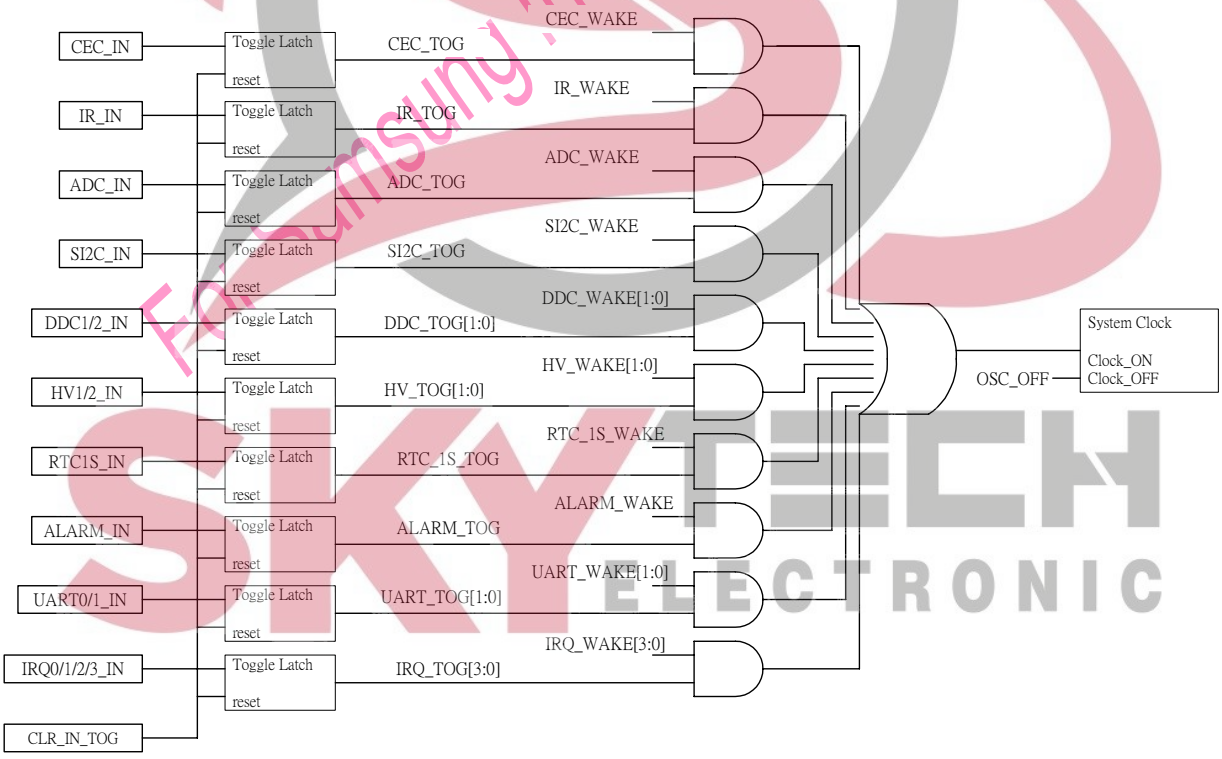
XTAL OSC=24MHz & XTAL_CLK=1: Don't use
XTAL OSC=12MHz & XTAL_CLK=0: Don't use

4.4. Wake-up & toggle Register

Index	Default	R/W	Bit	Name	Description
02	00	R/W	7	CEC_WAKE	1: MCU wake up by CEC 0: Disable MCU wake up by CEC
			6	IR_WAKE	1: MCU wake up by IR 0: Disable MCU wake up by IR
			5	ADC_WAKE	1: MCU wake up by Key pad ADC 0: Disable MCU wake up by Key pad ADC
			4	SI2C_WAKE	1: MCU wake up by slave IIC 0: Disable MCU wake up by slave IIC
			3	DDC_WAKE[1]	1: MCU wake up by 2nd DDC 0: Disable MCU wake up by 2nd DDC
			2	DDC_WAKE[0]	1: MCU wake up by 1st DDC 0: Disable MCU wake up by 1st DDC
			1	HV_WAKE[1]	1: MCU wake up by 2nd HV sync 0: Disable MCU wake up by 2nd HV sync
			0	HV_WAKE[0]	1: MCU wake up by 1st HV sync 0: Disable MCU wake up by 1st HV sync
03	00	R/W	7	RTC_1S_WAKE	1: MCU wake up by RTC 1s 0: Disable MCU wake up by RTC 1s
			6	ALARM_WAKE	1: MCU wake up by RTC alarm 0: Disable MCU wake up by RTC alarm
			5	UART_WAKE[1]	1: MCU wake up by UART1 0: Disable MCU wake up by UART1
			4	UART_WAKE[0]	1: MCU wake up by UART0 0: Disable MCU wake up by UART0
			3	IRQ_WAKE[3]	1: MCU wake up by IRQ[3] 0: MCU wake up by IRQ[3]
			2	IRQ_WAKE[2]	1: MCU wake up by IRQ[2] 0: MCU wake up by IRQ[2]
			1	IRQ_WAKE[1]	1: MCU wake up by IRQ[1] 0: MCU wake up by IRQ[1]
			0	IRQ_WAKE[0]	1: MCU wake up by IRQ[0] 0: MCU wake up by IRQ[0]
04	00	R	7	CEC_TOG	1: CEC toggle 0: No CEC toggle
		R	6	IR_TOG	1: IR toggle 0: No IR toggle
		R	5	ADC_TOG	1: Key pad ADC toggle 0: No Key pad ADC toggle
		R	4	SI2C_TOG	1: Slave IIC toggle 0: No slave IIC toggle
		R	3	DDC_ TOG[1]	1: 2nd DDC toggle 0: No 2nd DDC toggle
		R	2	DDC_ TOG[0]	1: 1st DDC toggle 0: No 1st DDC toggle
		R	1	HV_ TOG[1]	1: 2nd HV sync toggle 0: No 2nd HV sync toggle
		R	0	HV_ TOG[0]	1: 1st HV sync toggle 0: No 1st HV sync toggle
05	00	R	7	RTC_1S_TOG	1: RTC 1s toggle 0: No RTC 1s toggle
		R	6	ALARM_TOG	1: RTC alarm toggle 0: No RTC alarm toggle

		R	5	UART_TOG[1]	1: UART1 toggle 0: No UART1 toggle
		R	4	UART_TOG[0]	1: UART0 toggle 0: No UART0 toggle
		R	3	IRQ_ TOG[3]	1: IRQ[3] toggle 0: No IRQ[3] toggle
		R	2	IRQ_ TOG[2]	1: IRQ[2] toggle 0: No IRQ[2] toggle
		R	1	IRQ_ TOG[1]	1: IRQ[1] toggle 0: No IRQ[1] toggle
		R	0	IRQ_ TOG[0]	1: IRQ[0] toggle 0: No IRQ[0] toggle
06	00	W	7	CLR_IN_TOG	1: Clear all input Toggle 0: Disable clear all input Toggle
			6-0	Reserved	

(a) Power down procedure :
(1) Set RST_NDFILT=1,
(2) Disable watchdog timer reset
(3) Select wake up source
(4) Set OSC_OFF =1 & OSC_OFF =0
(5) Signals wake up MCU to MCU work : 16*12*1024*(Peripherals_clock)
If XTAL clock is 12MHz, and XTAL_CLK=1, Signals wake up MCU to MCU work:16.384ms



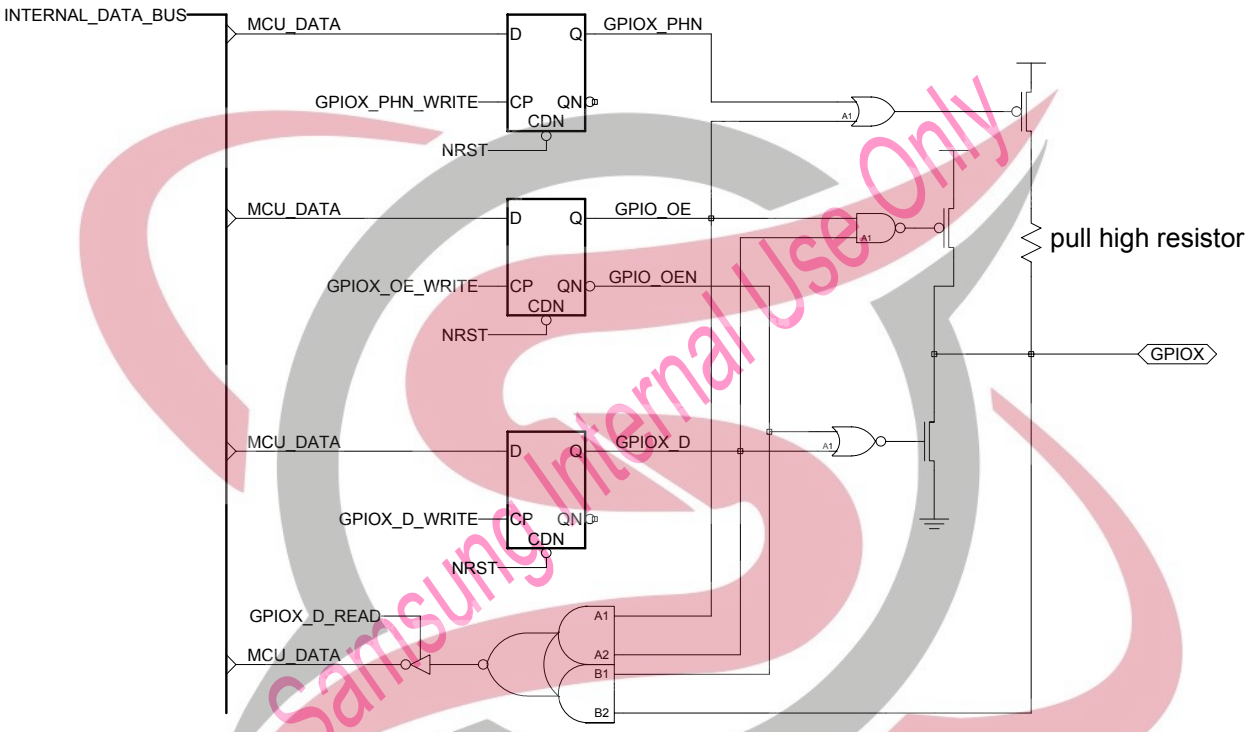
4.5. Watchdog Timer

Watchdog timer will generate a reset pulse if CPU does not write 08H register within 5.2s or 1s or 2s or 33ms or 65ms. This function can be disabled by setting DIS_WDT bit.

Index	Default	R/W	Bit	Name	Description
08	00	W	7	DIS_WDT	1: Disable Watchdog Timer 0: Enable Watchdog Timer
			6-3	Reserved	
			2-0	WDT[2:0]	000: reset time = 1s (default) 001: reset time = 2s 010: reset time = 33ms 011: reset time = 65ms 1xx: reset time = 5.2s

4.6. GPIO

The GPIOx0~ GPIOx7 are the general purpose IO shared with some special functions. When the special function is disabled, it is a general purpose I/O port. If it is configured as output, it could source/sink 4mA. If it is configured as input and GPIOx_PHN is “0”, it has an internal pull-up resistor. If the GPIOx is configured as input and the GPIOx_PHN is “1”, it doesn’t have an internal pull-up resistor.



Index	Default	R/W	Bit	Name	Description
10	00	R/W	7-6	Reserved	
			5-0	GPIOA_OE[5:0]	GPIO A output enable 1: output 0: input (default :input)
11	00	R/W	7	Reserved	
			6-0	GPIOB_OE[6:0]	GPIO B output enable 1: output 0: input
12	00	R/W	7-0	GPIOC_OE[7:0]	GPIO C output enable 1: output 0: input
13	00	R/W	7-0	GPIOD_OE[7:0]	GPIO D output enable 1: output 0: input
14	00	R/W	7-0	GPIOE_OE[7:0]	GPIO E output enable 1: output 0: input
15	00	R/W	7-6	Reserved	
			5-0	GPIOA_D[5:0]	Write : GPIO A output data Read : if GPIOA_OE=1, GPIO A output data if GPIOA_OE=0, GPIO A pin input data

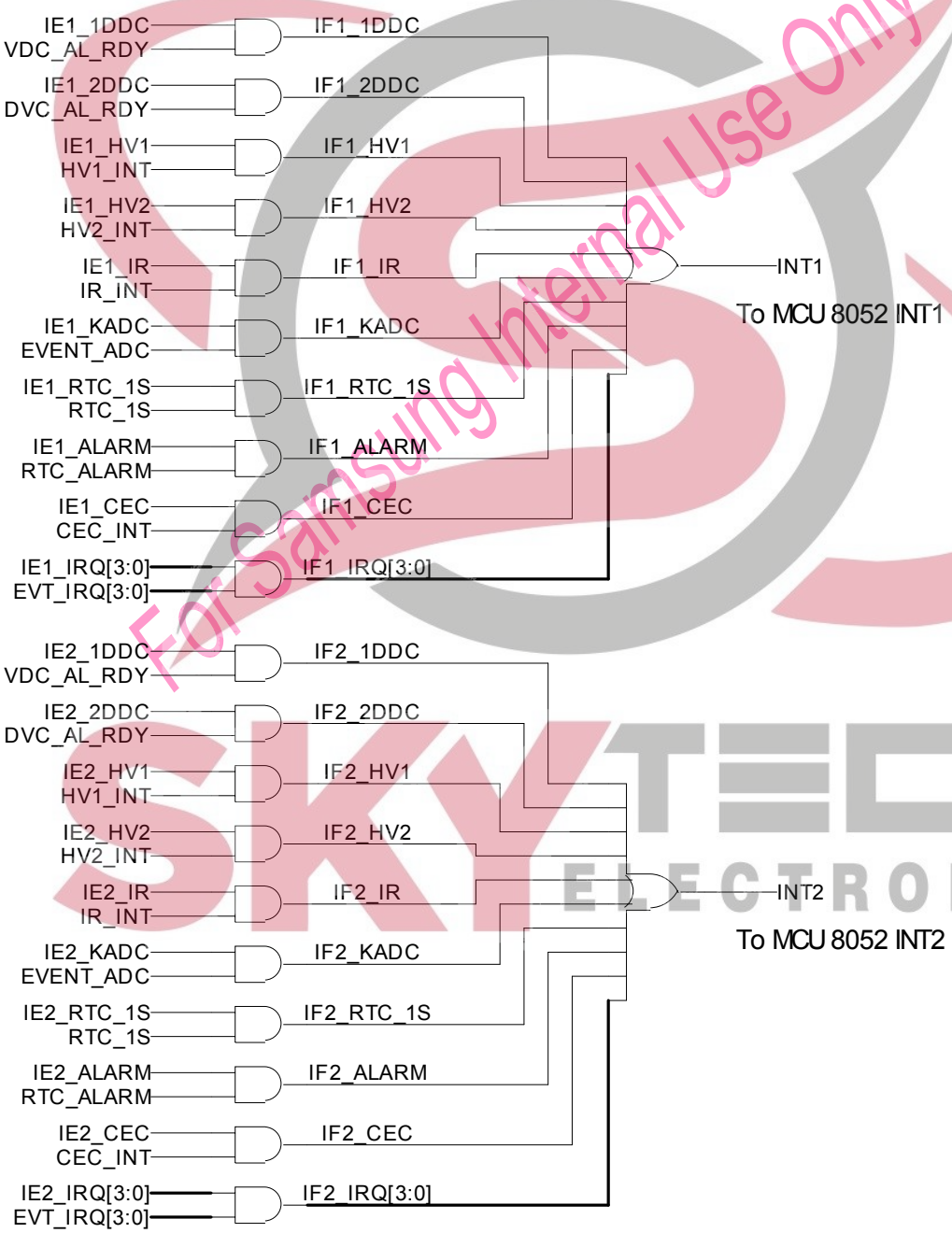
16	00	R/W	7	Reserved	
			6-0	GPIOB_D[6:0]	Write : GPIO B output data Read : if GPIOB_OE=1, GPIO B output data if GPIOB_OE=0, GPIO B pin input data
17	00	R/W	7-0	GPIOC_D[7:0]	Write : GPIO C output data Read : if GPIOC_OE=1, GPIO C output data if GPIOC_OE=0, GPIO C pin input data
18	00	R/W	7-0	GPIOD_D[7:0]	Write : GPIO D output data Read : if GPIOD_OE=1, GPIO D output data if GPIOD_OE=0, GPIO D pin input data
19	00	R/W	7-0	GPIOE_D[7:0]	Write : GPIO E output data Read : if GPIOE_OE=1, GPIO E output data if GPIOE_OE=0, GPIO E pin input data
1A	00	R/W	7-6	Reserved	
			5-0	GPIOA_PHN[5:0]	1: Disable GPIO A[x] pull high 0: Enable GPIO A[x] pull high
1B	00	R/W	7	Reserved	
			6-0	GPIOB_PHN[6:0]	1: Disable GPIO B[x] pull high 0: Enable GPIO B[x] pull high
1C	00	R/W	7-0	GPIOC_PHN[7:0]	1: Disable GPIO C[x] pull high 0: Enable GPIO C[x] pull high
1D	00	R/W	7-0	GPIOD_PHN[7:0]	1: Disable GPIO D[x] pull high 0: Enable GPIO D[x] pull high
1E	00	R/W	7-0	GPIOE_PHN[7:0]	1: Disable GPIO E[x] pull high 0: Enable GPIO E[x] pull high
20	00	R/W	7	EN_SLV_IO	1: Enable slave mode IIC IO pad 0: Disable slave mode IIC IO pad
			6	EN_UART0_IO	1: Enable UART0 IO pad 0: Disable UART0 IO pad
			5	EN_UART1_IO	1: Enable UART1 IO pad 0: Disable UART1 IO pad
			4	EN_CEC_IO	1: Enable CEC IO pad 0: Disable CEC IO PAD
			3	EN_2DDC_IO	1: Enable 2nd DDC IO pad 0: Disable 2nd DDC IO pad
			2	EN_LPWM_IO	1: Enable Low frequency PWM IO pad
			1-0	Reserved	
21	00	R/W	7-0	EN_P0_IO[7:0]	1: Enable 8052 P0[x] IO pad 0: Disable 8052 P0[x] IO pad
22	00	R/W	7-0	EN_P1_IO[7:0]	1: Enable 8052 P1[x] IO pad 0: Disable 8052 P1[x] IO pad
23	00	R/W	7-0	EN_AD_IO[7:0]	1: Enable ADC[x] IO pad 0: Disable ADC[x] IO pad
24	00	R/W	7-0	EN_PWM_IO[7:0]	1: Enable PWM[x] IO pad 0: Disable PWM[x] IO pad

4.7. 8052 Interrupt 1/2/3

INT1 is caused by 2 DDC or 2 HV DPMS detector or IR detector or key pad ADC, or RTC 1sec or alarm or 4 external IRQ or CEC. Each interrupt can be enabled/disabled independently by programming IE1_xxx register and identified by IF1_xxx register.

INT2 is caused by 2 DDC or 2 HV DPMS detector or IR detector or key pad ADC, or RTC 1sec or alarm or 4 external IRQ or CEC. Each interrupt can be enabled/disabled independently by programming IE2_xxx register and identified by IF2_xxx register.

INT3 is connect with SI2C interrupt



Interrupt1/2 Enable Register

Index	Default	R/W	Bit	Name	Description
30	00	R/W	7	IE1_1DDC	1: Enable 1st DDC interrupt 0: Disable 1st DDC interrupt
			6	IE1_2DDC	1: Enable 2nd DDC interrupt 0: Disable 2nd DDC interrupt
			5	IE1_HV1	1: Enable Hsync/Vsync detect I interrupt 0: Disable Hsync/Vsync detect I interrupt
			4	IE1_HV2	1: Enable Hsync/Vsync detect II interrupt 0: Disable Hsync/Vsync detect II interrupt
			3	IE1_IR	1: Enable IR detect interrupt 0: Disable IR detect interrupt
			2	IE1_KADC	1: Enable key pad ADC interrupt 0: Disable key pad ADC interrupt
			1	IE1_RTC_1S	1: Enable RTC 1s interrupt 0: Disable RTC 1s interrupt
			0	IE1_ALARM	1: Enable ALARM interrupt 0: Disable ALARM interrupt
31	00	R/W	7-5	Reserved	
			4	IE1_CEC	1: Enable CEC interrupt 0: Disable CEC interrupt
			3-0	IE1_IRQ[3:0]	1: Enable external IRQ[x] interrupt 0: Disable external IRQ[x] interrupt
32	00	R/W	7	IE2_1DDC	1: Enable 1st DDC interrupt 0: Disable 1st DDC interrupt
			6	IE2_2DDC	1: Enable 2nd DDC interrupt 0: Disable 2nd DDC interrupt
			5	IE2_HV1	1: Enable Hsync/Vsync detect I interrupt 0: Disable Hsync/Vsync detect I interrupt
			4	IE2_HV2	1: Enable Hsync/Vsync detect II interrupt 0: Disable Hsync/Vsync detect II interrupt
			3	IE2_IR	1: Enable IR detect interrupt 0: Disable IR detect interrupt
			2	IE2_KADC	1: Enable key pad ADC interrupt 0: Disable key pad ADC interrupt
			1	IE2_RTC_1S	1: Enable RTC 1s interrupt 0: Disable RTC 1s interrupt
			0	IE2_ALARM	1: Enable ALARM interrupt 0: Disable ALARM interrupt
33	00	R/W	7-5	Reserved	
			4	IE2_CEC	1: Enable CEC interrupt 0: Disable CEC interrupt
			3-0	IE2_IRQ[3:0]	1: Enable external IRQ[x] interrupt 1: Disable external IRQ[x] interrupt

Interrupt1/2 Flag Register

Index	Default	R/W	Bit	Name	Description
34	00	R	7	IF1_1DDC	1: Event of 1st DDC interrupt 0: No event of 1st DDC interrupt
			6	IF1_2DDC	1: Event of 2nd DDC interrupt 0: No event of 2nd DDC interrupt
			5	IF1_HV1	1: Event of Hsync/Vsync detect I interrupt 0: No event of Hsync/Vsync detect I interrupt
			4	IF1_HV2	1: Event of Hsync/Vsync detect II interrupt 0: No event of Hsync/Vsync detect II interrupt
			3	IF1_IR	1: Event of IR detect interrupt

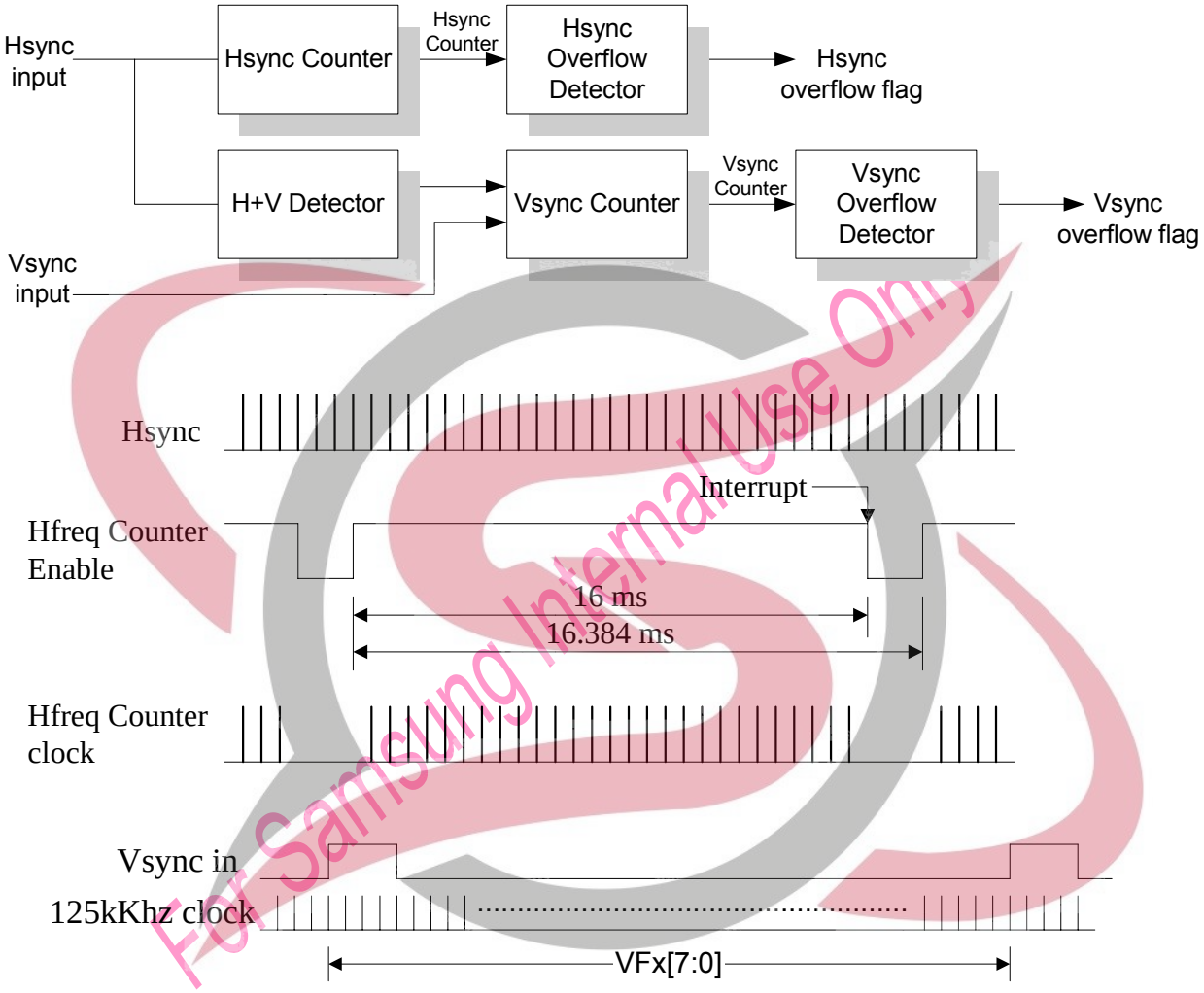
					0: No event of IR detect interrupt
			2	IF1_KADC	1: Event of key pad ADC interrupt 0: No event of key pad ADC interrupt
			1	IF1_RTC_1S	1: Event of RTC 1s interrupt 0: No event of RTC 1s interrupt
			0	IF1_ALARM	1: Event of ALARM interrupt 0: No event of ALARM interrupt
35	00	R	7-5	Reserved	
			4	IF1_CEC	1: Event of CEC interrupt 0: No event of CEC interrupt
			3	IF1_IRQ[3]	1: Event of external IRQ[3] interrupt 0: No event of external IRQ[3] interrupt
			2	IF1_IRQ[2]	1: Event of external IRQ[2] interrupt 0: No event of external IRQ[2] interrupt
			1	IF1_IRQ[1]	1: Event of external IRQ[1] interrupt 0: No event of external IRQ[1] interrupt
			0	IF1_IRQ[0]	1: Event of external IRQ[0] interrupt 0: No event of external IRQ[0] interrupt
36	00	R	7	IF2_1DDC	1: Event of 1st DDC interrupt 0: No event of 1st DDC interrupt
			6	IF2_2DDC	1: Event of 2nd DDC interrupt 0: No event of 2nd DDC interrupt
			5	IF2_HV1	1: Event of Hsync/Vsync detect I interrupt 0: No event of Hsync/Vsync detect I interrupt
			4	IF2_HV2	1: Event of Hsync/Vsync detect II interrupt 0: No event of Hsync/Vsync detect II interrupt
			3	IF2_IR	1: Event of IR detect interrupt 0: No event of IR detect interrupt
			2	IF2_KADC	1: Event of key pad ADC interrupt 0: No event of key pad ADC interrupt
			1	IF2_RTC_1S	1: Event of RTC 1s interrupt 0: No event of RTC 1s interrupt
			0	IF2_ALARM	1: Event of ALARM interrupt 0: No event of ALARM interrupt
37	00	R	7-5	Reserved	
			4	IF1_CEC	1: Event of CEC interrupt 0: No event of CEC interrupt
			3	IF2_IRQ[3]	1: Event of external IRQ[3] interrupt 0: No event of external IRQ[3] interrupt
			2	IF2_IRQ[2]	1: Event of external IRQ[2] interrupt 0: No event of external IRQ[2] interrupt
			1	IF2_IRQ[1]	1: Event of external IRQ[1] interrupt 0: No event of external IRQ[1] interrupt
			0	IF2_IRQ[0]	1: Event of external IRQ[0] interrupt 0: No event of external IRQ[0] interrupt

4.8. External IRQ Interrupt

IRQ Polling Flag Register

Index	Default	R/W	Bit	Name	Description
3A	00	R	7-4	EVT_IRQ[3:0]	1: Event of external IRQ[x] 0: No event of external IRQ[x]
		W	3-0	CLR_IRQ[3:0]	1: Clear event of external IRQ[x] 0: No clear event of external IRQ[x]
3B	00	R/W	7-4	IRQ_CHG[3:0]	1: Rising & falling trigger 0: Single edge trigger
			3-0	IRQ_EDGE[3:0]	1: Falling trigger 0: Rising trigger

4.9. HV Sync DPMS Detector



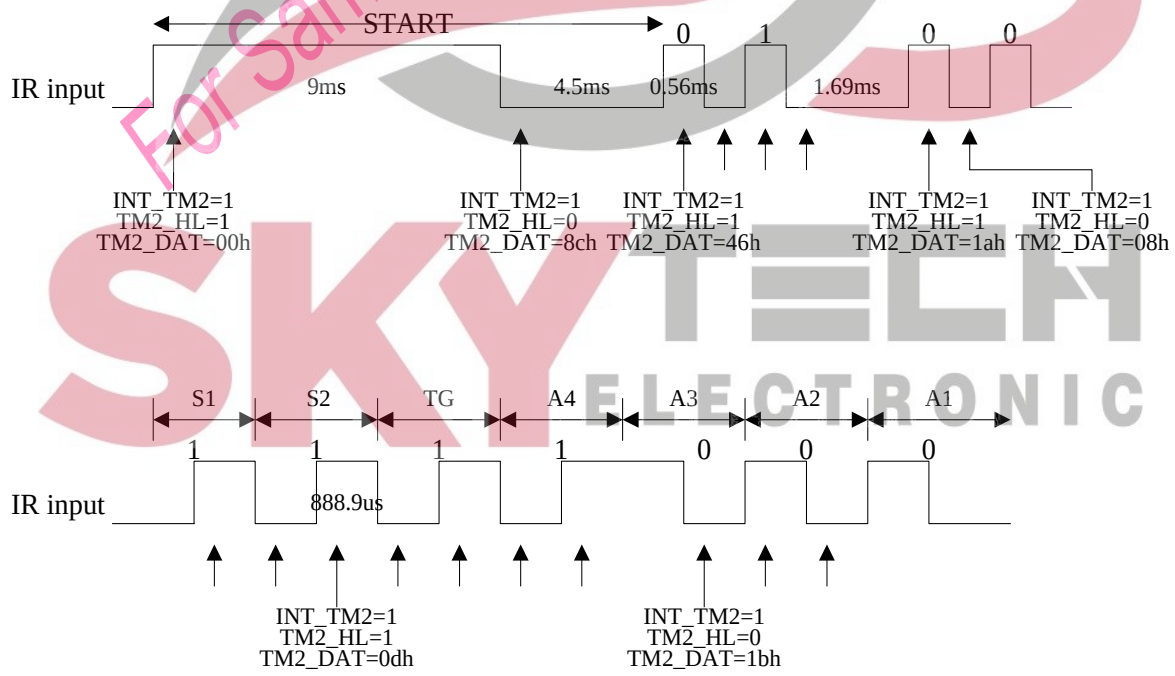
Index	Default	R/W	Bit	Name	Description
40	00	R/W	7	EN_HV1_CNT	1: Enable HV1 detection count 0: Disable HV1 detection count
			6	EN_VIN1_INT	1: Enable VSYNC1 input interrupt 0: Disable VSYNC1 input interrupt
			5	EN_H16M1_INT	1: Enable HSYNC1 16ms interrupt 0: Disable HSYNC1 16ms interrupt
			4	EN_V1OV_INT	1: Enable V1 overflow interrupt 0: Disable V1 overflow interrupt
			3	EN_H1OV_INT	1: Enable H1 overflow interrupt 0: Disable H1 overflow interrupt
			2-0	Reserved	
41	00	R	7	HV1_INT	1: Event HV1 interrupt (HV1 “OR”) 0: No event HV1 interrupt
			6	VIN1_INT	1: VSYNC1 input interrupt (rising edge trigger) 0: No VSYNC1 input interrupt
			5	HIN1_INT	1: HSYNC1 16ms interrupt

					0: No HSYNC1 16ms interrupt
			4	V1_OVRFL	1: V1 overflow interrupt 0: No V1 overflow interrupt
			3	H1_OVRFL	1: H1 overflow interrupt 0: No H1 overflow interrupt
			2-0	Reserved	
42	00	W	7	CLR_VIN1_INT	1: Clear VSYN1 input interrupt 0: No clear VSYN1 input interrupt
			6	CLR_HIN1_INT	1: Clear HSYN1 16ms interrupt 0: No clear HSYN1 16ms interrupt
			5	CLR_V1OV_INT	1: Clear V1 overflow interrupt 0: No clear V1 overflow interrupt
			4	CLR_H1OV_INT	1: Clear H1 overflow interrupt 0: No clear H1 overflow interrupt
		R	3	HV1_COMP	1: Detect H1+V1 0: No detect H1+V1
		R/W	2	EN_HV1_COMP	1: Enable H1+V1 mode (H+V from HIN1 pin) 0: Disable H1+V1 mode
		R/W	1-0	H1_LWP[1:0]	H1+V1 low pass filter pulse width =00 : 8us (default) =01 : 4us =10 : 16us =11 : 32us
43	00	R	7-4	Reserved	
			3-0	HF1[3:0]	H1 counter in 16ms period
44	00	R	7-0	HF1[11:4]	
45	00	R/W	7-0	H1_LOV[7:0]	Low H1 overflow count (compare with HF1[11:4])
46	00	R	7-6	Reserved	
			5-0	VF1[5:0]	125khz counter in V1 period
47	00	R	7-0	VF1[13:6]	
48	FF	R/W	7-0	V1_LOV[7:0]	Low V1 overflow count(compare with VF1[13:6])
50	00	R/W	7	EN_HV2_CNT	1: Enable HV2 detection count 0: Disable HV2 detection count
			6	EN_VIN2_INT	1: Enable VSYNC2 input interrupt 0: Disable VSYNC2 input interrupt
			5	EN_H16M2_INT	1: Enable HSYNC2 16ms interrupt 0: Disable HSYNC2 16ms interrupt
			4	EN_V2OV_INT	1: Enable V2 overflow interrupt 0: Disable V2 overflow interrupt
			3	EN_H2OV_INT	1: Enable H2 overflow interrupt 0: Disable H2 overflow interrupt
			2-0	Reserved	
51	00	R	3	HV2_INT	1: Event HV2 interrupt(HV2 “OR”) 0: No event HV2 interrupt
			2	VIN2_INT	1: VSYNC2 input interrupt (rising edge trigger) 0: No VSYNC2 input interrupt
			5	HIN2_INT	1: HSYNC2 16ms interrupt 0: No HSYNC2 16ms interrupt
			1	V2_OVRFL	1: V2 overflow interrupt 0: No V2 overflow interrupt
			0	H2_OVRFL	1: H2 overflow interrupt 0: No H2 overflow interrupt
			2-0	Reserved	
52	00	W	7	CLR_VIN2_INT	1: Clear VSYN2 input interrupt 0: No clear VSYN2 input interrupt
			6	CLR_HIN2_INT	1: Clear HSYN2 16ms interrupt

					0: No clear HSYN2 16ms interrupt
			5	CLR_V2OV_INT	1: Clear V2 overflow interrupt 0: No clear V2 overflow interrupt
			4	CLR_H2OV_INT	1: Clear H2 overflow interrupt 0: No clear H2 overflow interrupt
		R	3	HV2_COMP	1: Detect H2+V2 0: No detect H2+V2
		R/W	2	EN_HV2_COMP	1: Enable H2+V2 mode(H+V from HIN2 pin) 0: Disable H2+V2 mode
		R/W	1-0	H2_LWP[1:0]	H2+V2 low pass filter pulse width =00 : 8us (default) =01 : 4us =10 : 16us =11 : 32us
53	00	R	7-4	Reserved	
			3-0	HF2[3:0]	H2 counter in 16ms period
54	00	R	7-0	HF2[11:4]	
55	00	R/W	7-0	H2_LOV[7:0]	Low H2 overflow count (compare with HF2[11:4])
56	00	R	7-6	Reserved	
			5-0	VF2[5:0]	125khz counter in V2 period
57	00	R	7-0	VF2[13:6]	
58	FF	R/W	7-0	V2_LOV[7:0]	Low V2 overflow count(compare with VF2[13:6])

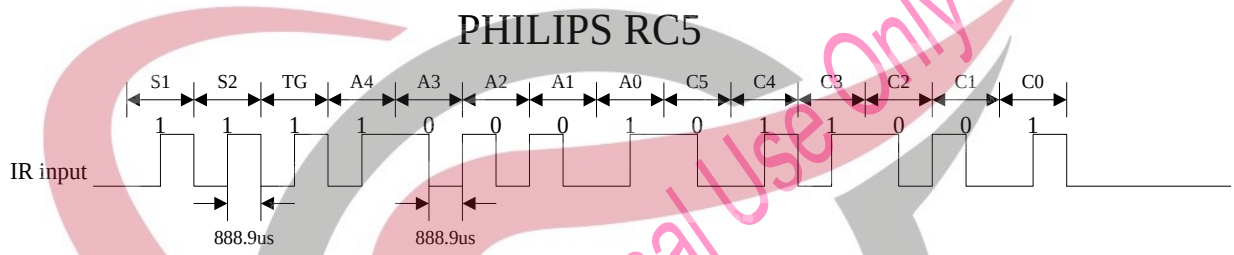
4.10. Remote Control

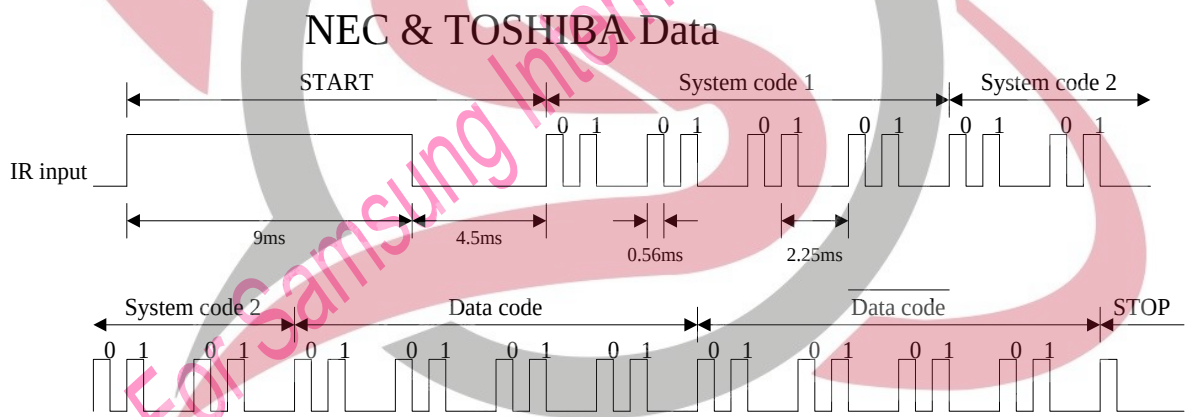
Index	Default	R/W	Bit	Name	Description
60	00	R/W	7	EN_IR	1:Enable IR 0:Disable IR
			6	IR_SEDG	1:Single edge trigger 0:Both edge trigger
			5	IR_RF	1:Rising edge trigger 0:Falling edge trigger
			4	EN_OV_INT	1:Enable over flow interrupt 0:Disable over flow interrupt
			3-2	PRE_SCAL[1:0]	Pre scaler time 00:64us 01:32us 10:128us 11:1ms
			1	CLR_IR_INT	1:Clear interrupt "IR_INT 0:No clear interrupt "IR_INT
			0	Reserved	
61	04	R	7-3	Reserved	
			2	IR_HL	Read IR input H/L
			1	IR_OVFLW	1:IR over flow interrupt 0:No IR over flow interrupt
			0	IR_INT	1: IR interrupt = edge trigger + over flow 0:No IR interrupt
62	00	R	7-0	IR_CNT[7:0]	IR counter low byte

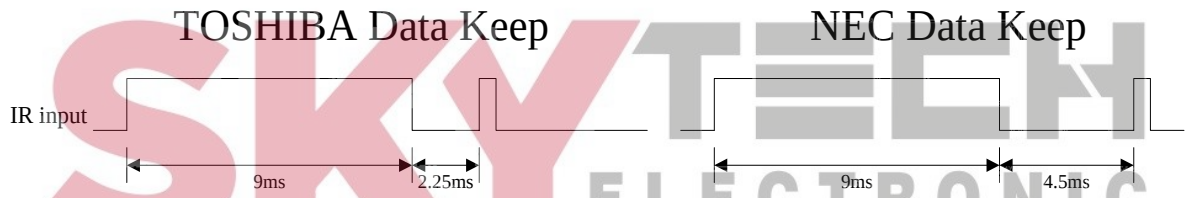


IR Timing Table

		STARTH	STARTL	pulse	H period	L period
TC9290	data	9	4.5	0.56	2.25	1.125
(TC9243)	keep	9	4.5	0.56	2.25	
NEC uPD6P5	data	9	4.5	0.56	2.25	1.125
	keep	9	2.25	0.56		
Philips RC5	data	0.889	0.889	0.889	0.889	0.889

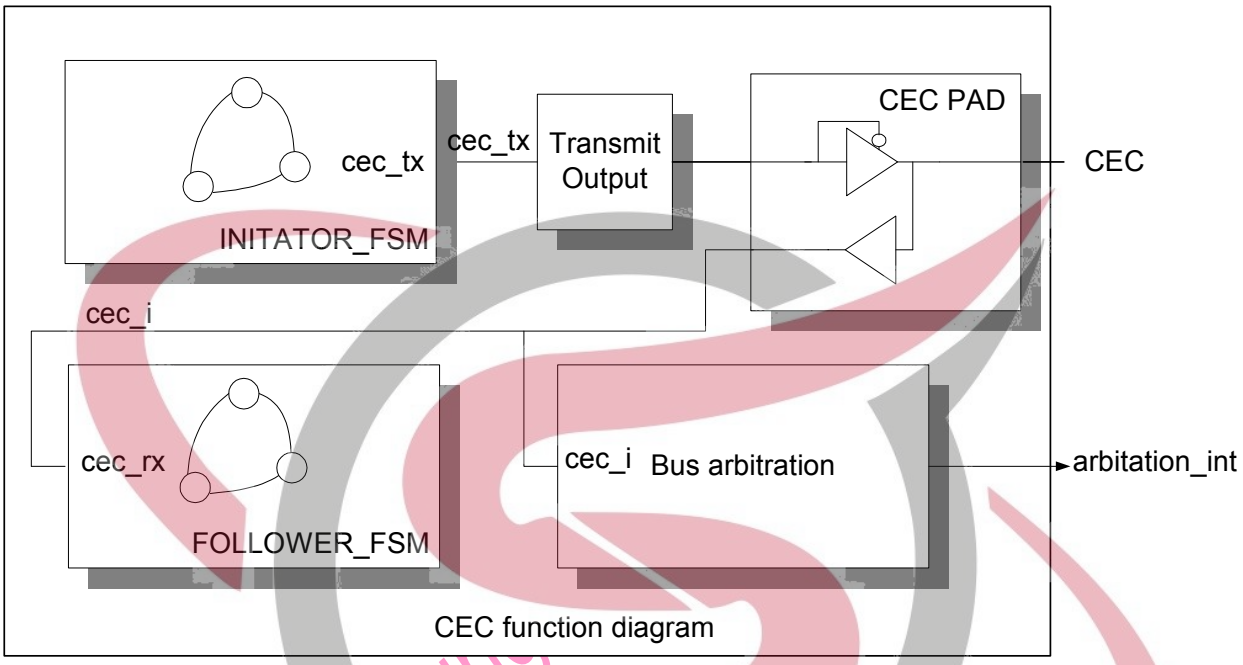






4.11. HDMI CEC Control

Receive/Transmit data flow:



4.11.1. HDMI CEC CONTROL & DATA REGISTER

Control

Index	Default	R/W	Bit	Name	Description
70	00	R/W	7	EN_CEC	1: Enable HDMI CEC 0: Disable HDMI CEC
			6-5	Reserved	
		R	4	CEC_BUSY	1: CEC line busy 0: CEC line no busy
			3	Reserved	
		W	2	CEC_L_3600US	1: Force CEC line= “L” 3.6ms 0: Disable force CEC line= “L” 3.6ms
			1-0	Reserved	

EN_CEC =0, will force state to IDLE.

Initiator

Index	Default	R/W	Bit	Name	Description
71	20	R/W	7	CEC_TR	1: Enable initiator state and transmit data 0: Follower state
		R/W	6	CEC_O_EOM	EOM bit
		R	5	CEC_RXACK	1: NACK 0: Receive ACK
			4-0	Reserved	

Follower

Index	Default	R/W	Bit	Name	Description
72	00	R	7	CEC_I_STR	1: Receive START Phase 0: No START Phase
		R	6	CEC_I_EOM	1: EOM=1 0: EOM=0
		R/W	5	CEC_TXACK	1: Transmit NACK 0: Transmit ACK
		R/W	4	CEC_NACK_INT	When NACK, next RX_INT will be set.
			3-0	Reserved	

Clear CEC_I_STR by (CLR_RX_INT or CLR_TX_INT) register to write 1.

Interrupt & Clear Interrupt

Index	Default	R/W	Bit	Name	Description
73	00	R	7	CEC_INT	1: Event CEC interrupt "OR" (tx_int, rx_int, dloss, tm_out, line_error) 0: No event CEC interrupt
			6	CEC_TX_INT	1: Event transmit interrupt (after time of data bit) 0: No event transmit interrupt
			5	CEC_RX_INT	1: Event receive interrupt (after time of data bit) 0: No event receive interrupt
			4	CEC_DLOSS	1: Event arbitrate loss interrupt(Note 2) 0: No event arbitrate loss interrupt
			3	CEC_TM_OUT	1: Event time out interrupt 0: No event time out interrupt
			2	CEC_LINE_ERROR	1: Event LINE error interrupt (Note 3) 0: No event LINE error interrupt
			1-0	Reserved	
74	00	W	7	Reserved	
			6	CLR_TX_INT	1: Clear transmit interrupt 0: No clear transmit interrupt
			5	CLR_RX_INT	1: Clear receive interrupt 0: No clear receive interrupt
			4	CLR_DLOSS	1: Clear arbitrate loss interrupt 0: No clear arbitrate loss interrupt
			3	CLR_ TM_OUT	1: Clear time out interrupt 0: No clear time out interrupt
			2	CLR_ LINE_ERROR	1: Clear line error interrupt 0: No clear line error interrupt
			1-0	Reserved	

Note 1. Clear interrupt need to write 1

Note 2. The initiator monitor the CEC line and if whilst in high impedance state it detects low impedance then it shall assume that it has lost the arbitration. Then the CEC_DLOSS will be set and CEC_TR will be clear. Then the device will stop transmitting and become a follower.
If CEC_DLOSS has been set,
1. Force state to IDLE. (Clear EN_CEC, and re-set EN_CEC)
2. Initiator wants to re-send data, need to wait "signal free time" (MARK 1) and re-set CEC_TR.

Note 3. It is the responsibility of all devices acting has follows to detect the existence of spurious pulses on the control signal line and notify all other device (primarily the initiator that a potential error has occurred.
If CEC_LINE_ERROR flag have been set
1. Set CEC_L_3600US
2. Force state to IDLE.(Clear EN_CEC, and re-set EN_CEC)

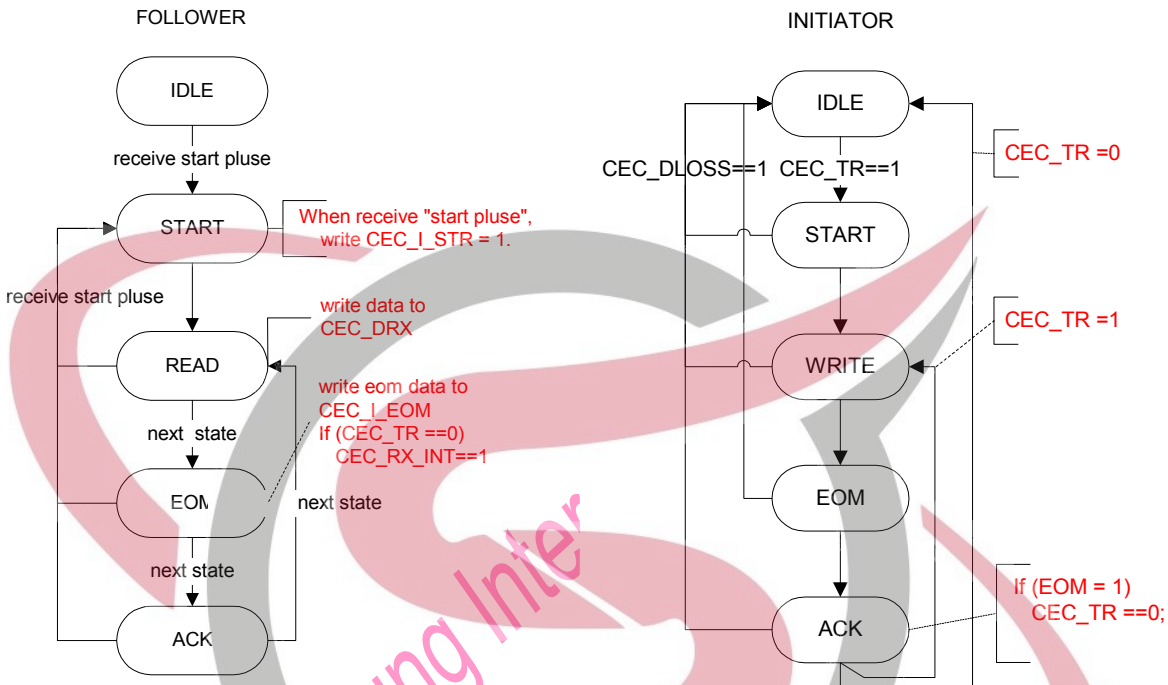
Transmit/Receive buffer

Index	Default	R/W	Bit	Name	Description
75	FF	R/W	7-0	CEC_DTX[7:0]	CEC transmit buffer
76	00	R	7-0	CEC_DRX[7:0]	CEC receive buffer

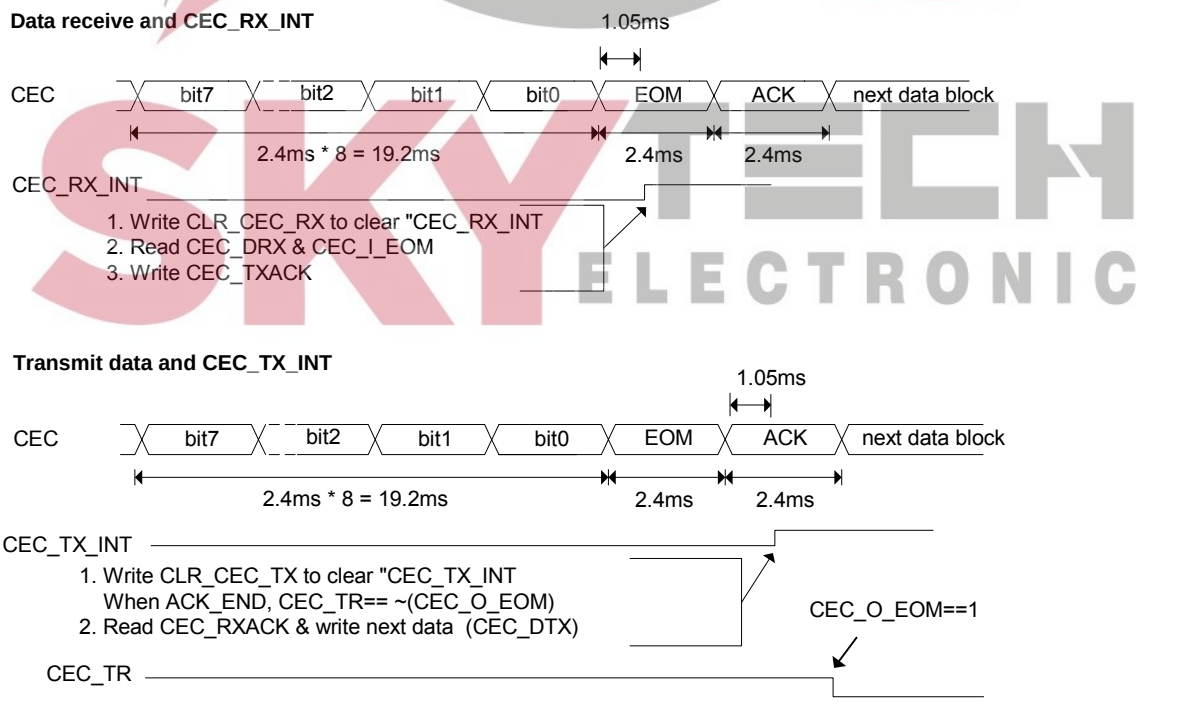
Mark 1: CEC Table Signal Free Time

Precondition	Signal Free Time (nominal data bit periods)
Present initiator wants to send another frame immediately after its previous frame	≥7 and <10
New initiator wants to send a frame	≥5 and <7
Previous attempt to send frame unsuccessful	≥3 and <5

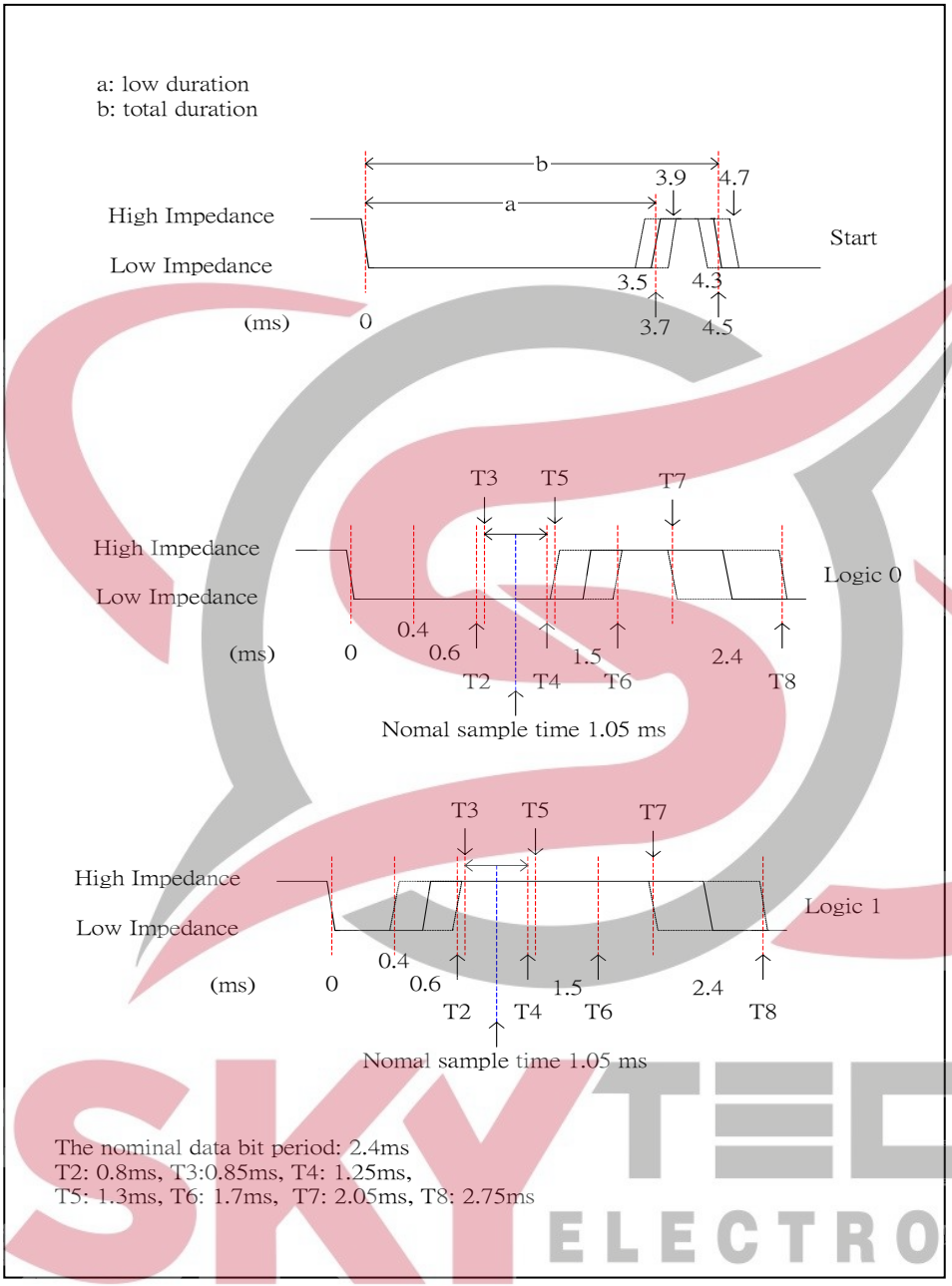
4.11.2. FOLLOWER AND INITIATOR FUNCTION DIAGRAM



4.11.3. CEC_RX_INT AND CEC_TX_INT TIMING



4.11.4. BIT TIMING (START AND DATA BITS)

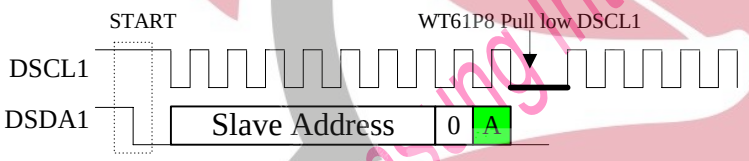


4.12. VGA/DVI DDC

VGA DDC Control Register (1st DDC)

Index	Default	R/W	Bit	Name	Description
80	00	R/W	7	VDC_EN_DDC	1: Enable VGA DDC function. 0: Disable VGA DDC function. Clearing VDC_EN_DDC is to reset VGA DDC H/W.
			6	VDC_CLR_RT	1: Clear transmit/receive interrupt 0: No clear transmit/receive interrupt
			5	VDC_CLR_STP	1: Clear STOP phase interrupt 0: No clear STOP phase interrupt
			4	VDC_WAIT(1)	1: Enable pull low DSCL1 when 9th DSCL1 bit 0: Disable pull low DSCL1 when 9th DSCL1 bit This bit is to handshake 9th DSCL1 bit between master IIC and slave IIC
			3	VDC_ENADR8 (2)	1: don't compare VDC_SADR1[3:1] for DDC 0: DDC slave address need to match VDC_SADR1 [6:0]
			2-1	Reserved	
			0	VDC_TXNAK	1: Transmit NACK when WRITE phase 0: Transmit ACK when WRITE phase

(1) If IIC speed is over F/W process data time, F/W have to set "VDC_WAIT". WT61P8 pulls low 9th DSCL1 and handshakes master IIC (host)



(2) If VDC_ENADR8=1, WT61P8 compares received slave address with VDC_SADR1[7:4]
For example : If VDC_ENADR8=1 and VDC_SADR1="A1". WT61P8 can be interrupted by slave address = A0,A1,A2,A3…AF

VGA DDC Status Register (1st DDC)

Index	Default	R/W	Bit	Name	Description
81	00	R	7	VDC_AL_RDY	1: Event interrupt from VDC_INT_RT or VDC_INT_STOP 0: No interrupt from VDC_INT_RT or VDC_INT_STOP
			6	VDC_INT_RT	1: Receive/transmit slave I or II data interrupt (9th DSCL1) 0: No receive/transmit slave I or II data interrupt (9th DSCL1)
			5	VDC_INT_STOP	1: Event "STOP" phase interrupt 0: No "STOP" phase interrupt
			4-3	Reserved	
			2	VDC_FIRST	1: In "FIRST" phase 0: Not in "FIRST" phase
			1	VDC_ALRW	1: In "RAED" phase 0: In "WRITE" phase
			0	VDC_RXNAK	Receive ACK bit 1: NACK 0: ACK
82	00	R	7-3	Reserved	
			2	VDC_BB	1: DSCL1 & DSDA1 Bus busy 0: DSCL1 & DSDA1 Bus no busy
			1	VDC_SLV2	1: Receive Slave address2

					0: No receive Slave address2
			0	VDC_SLV1	1: Receive Slave address 1 0: No receive Slave address 1

VGA DDC Slave I II Receive & Transmit Buffer Register (1st DDC)

Index	Default	R/W	Bit	Name	Description
83	FF	R/W	7-0	VDC_DTX1[7:0]	Slave 1 transmit buffer
84	FF	R/W	7-0	VDC_DTX2[7:0]	Slave 2 transmit buffer
85	00	R	7-0	VDC_DRX[7:0]	Slave 1,2, receive buffer

VGA DDC Slave Address Register (1st DDC)

Index	Default	R/W	Bit	Name	Description
86	00	R/W	7-1	VDC_SADR1[6:0]	Slave 1 address
			0	VDC_EN_SA1	1: Enable Slave address 1 VDC_SADR1[6:0] compare 0: Disable Slave address 1 VDC_SADR1[6:0] compare
87	00	R/W	7-1	VDC_SDAR2[6:0]	Slave 2 address
			0	VDC_EN_SA2	1: Enable Slave address 2 VDC_SADR2[6:0] compare 0: Disable Slave address 2 VDC_SADR2[6:0] compare

DVI DDC Control Register (2nd DDC)

Index	Default	R/W	Bit	Name	Description
90	00	R/W	7	DVC_EN_DDC	1: Enable DVI DDC function. 0: Disable DVI DDC function. Clearing DVC_EN_DDC is to reset DVI DDC H/W.
			6	DVC_CLR_RT	1: Clear transmit/receive interrupt 0: No clear transmit/receive interrupt
			5	DVC_CLR_STP	1: Clear STOP phase interrupt 0: No clear STOP phase interrupt
			4	DVC_WAIT	1: Enable pull low DSCL2 when 9th DSCL2 bit 0: Disable pull low DSCL2 when 9th DSCL2 bit This bit is to handshake 9th SCL bit between master IIC and slave IIC
			3	DVC_ENADR8	1: don't compare DVC_SADR1[3:1] for DDC 0: DDC slave address need to match DVC_SADR1 [6:0]
			2-1	Reserved	
			0	DVC_TXNAK	Transmit ACK bit 1: NACK 0: ACK

DVI DDC Status Register (2nd DDC)

Index	Default	R/W	Bit	Name	Description
91	00	R	7	DVC_AL_RDY	1: Event interrupt from DVC_INT_RT or DVC_INT_STOP 0:No interrupt from DVC_INT_RT or DVC_INT_STOP
			6	DVC_INT_RT	1: Receive/transmit slave I or II data interrupt (9th DSCL2) 0: No receive/transmit slave I or II data interrupt (9th DSCL2)
			5	DVC_INT_STOP	1: Event "STOP" phase interrupt 0: No "STOP" phase interrupt
			4-3	Reserved	
			2	DVC_FIRST	1: In "FIRST" phase 0: Not in "FIRST" phase
			1	DVC_ALRW	1: In "RAED" phase 0: In "WRITE" phase

			0	DVC_RXNAK	receive ACK bit 1: NACK 0: ACK
92	00	R	7-3	Reserved	
			2	DVC_BB	1: DSCL2 & DSDA2 Bus busy 0: DSCL2 & DSDA2 Bus no busy
			1	DVC_SLV2	1: Receive Slave address2 0: No receive Slave address2
			0	DVC_SLV1	1: Receive Slave address 1 0: No receive Slave address 1

DVI DDC Slave I II Receive & Transmit Buffer Register (2nd DDC)

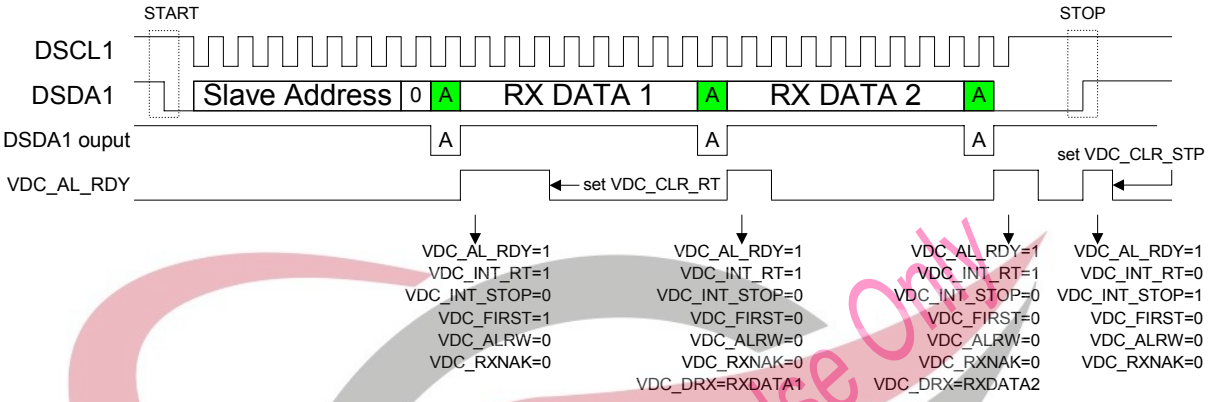
Index	Default	R/W	Bit	Name	Description
93	FF	R/W	7-0	DVC_DTX1[7:0]	Slave 1 transmit buffer
94	FF	R/W	7-0	DVC_DTX2[7:0]	Slave 2 transmit buffer
95	00	R	7-0	DVC_DRX[7:0]	Slave 1,2, receive buffer

Index	Default	R/W	Bit	Name	Description
96	00	R/W	7-1	DVC_SADR1[6:0]	Slave 1 address
			0	DVC_EN_SA1	1: Enable Slave address 1 DVC_SADR1[6:0] compare 0: Disable Slave address 1 DVC_SADR1[6:0] compare
97	00	R/W	7-1	DVC_SDAR2[6:0]	Slave 2 address
			0	DVC_EN_SA2	1: Enable Slave address 2 DVC_SADR2[6:0] compare 0: Disable Slave address 2 DVC_SADR2[6:0] compare

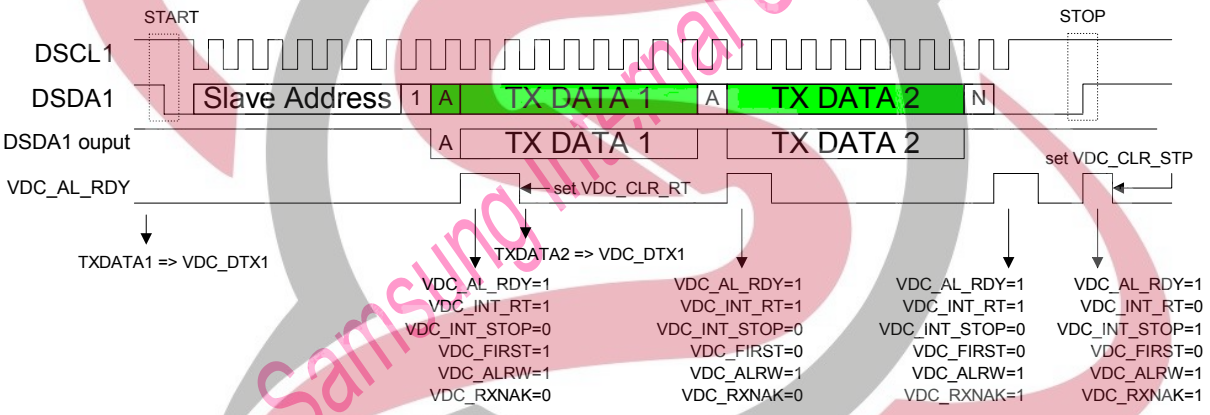
DVI DDC Slave Address Register (2nd DDC)

WT61P8 VGA/DVI DDC Data Flow

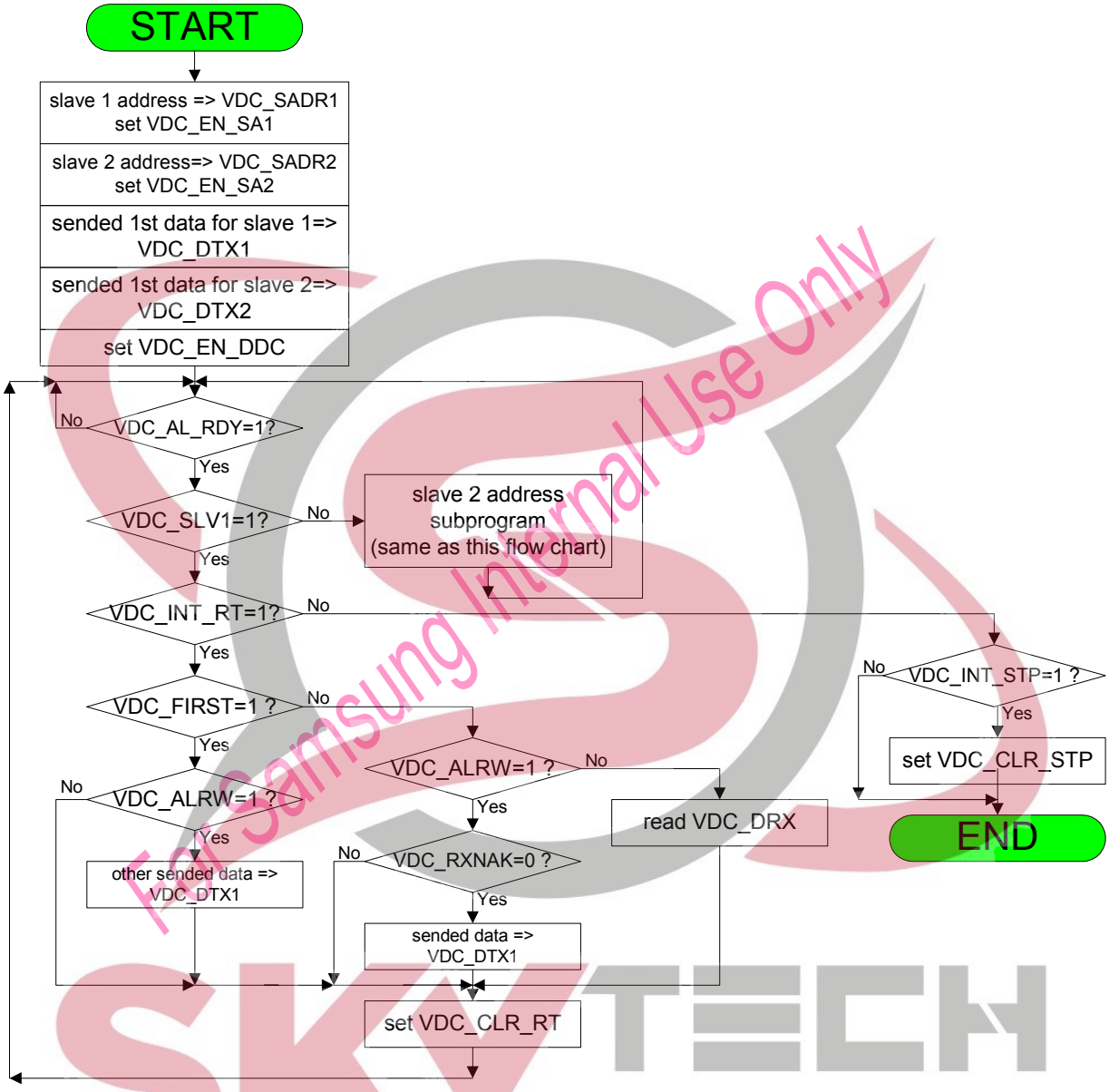
(1) DDC2 slave I,II write mode :



(2) DDC2 slave I,II read mode :



WT61P8 DDC Flow Chart



4.13. Slave I²C Interface

Slave IIC Control Register

Index	Default	R/W	Bit	Name	Description
A0	00	R/W	7	IIC_EN_IIC	1: Enable slave IIC function. 0: Disable slave IIC function. Clearing IIC_EN_IIC is to reset SIIC H/W.
			6	IIC_CLR_RT	1: Clear transmit/receive interrupt 0: No clear transmit/receive interrupt
			5	IIC_CLR_STP	1: Clear STOP phase interrupt 0: No clear STOP phase interrupt
			4	IIC_WAIT(1)	1: Enable pull low SSCL when 9th SSCL bit 0: Disable pull low SSCL when 9th SSCL bit This bit is to handshake 9th SCL bit between master IIC and slave IIC
			3-1	Reserved	
			0	IIC_TXNAK	1: Transmit NACK when WRITE phase 0: Transmit ACK when WRITE phase

(1) If IIC speed is over F/W process data time, F/W have to set "IIC_WAIT". WT61P8 pulls low 9th SSCL and handshakes master IIC (host)

Slave IIC Status Register

Index	Default	R/W	Bit	Name	Description
A1	00	R	7	IIC_AL_RDY	1: Event interrupt from IIC_INT_RT or IIC_INT_STOP 0: No interrupt from IIC_INT_RT or IIC_INT_STOP
			6	IIC_INT_RT	1: Receive/transmit data interrupt (9th SSCL) 0: No receive/transmit data interrupt (9th SSCL)
			5	IIC_INT_STOP	1: Event "STOP" phase interrupt 0: No "STOP" phase interrupt
			4-3	Reserved	
			2	IIC_FIRST	1: In "FIRST" phase 0: Not in "FIRST" phase
			1	IIC_ALRW	1: In "READ" phase 0: In "WRITE" phase
			0	IIC_RXNAK	receive ACK bit 1: NACK 0: ACK

Slave IIC Slave I II Receive & Transmit Buffer Register

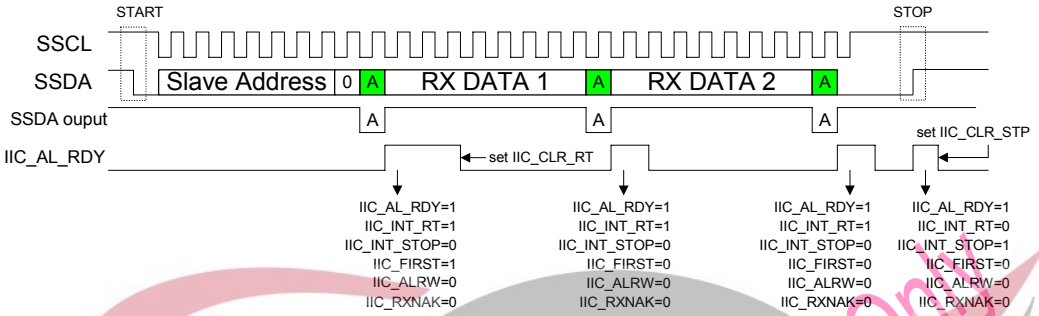
Index	Default	R/W	Bit	Name	Description
A2	FF	R/W	7-0	IIC_DTX1[7:0]	Slave 1 transmit buffer
A3	00	R	7-0	IIC_DRX[7:0]	Slave 1,2, receive buffer

Slave IIC Slave Address Register

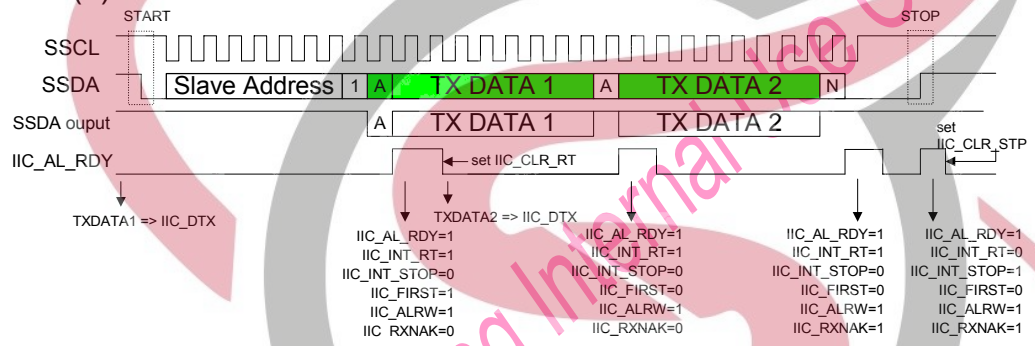
Index	Default	R/W	Bit	Name	Description
A4	00	R/W	7-1	IIC_SADR[6:0]	Slave address
			0	IIC_EN_SA	1: Enable Slave address IIC_SADR[6:0] compare 0: Disable Slave address IIC_SADR[6:0] compare

WT61P8 Slave IIC Data Flow

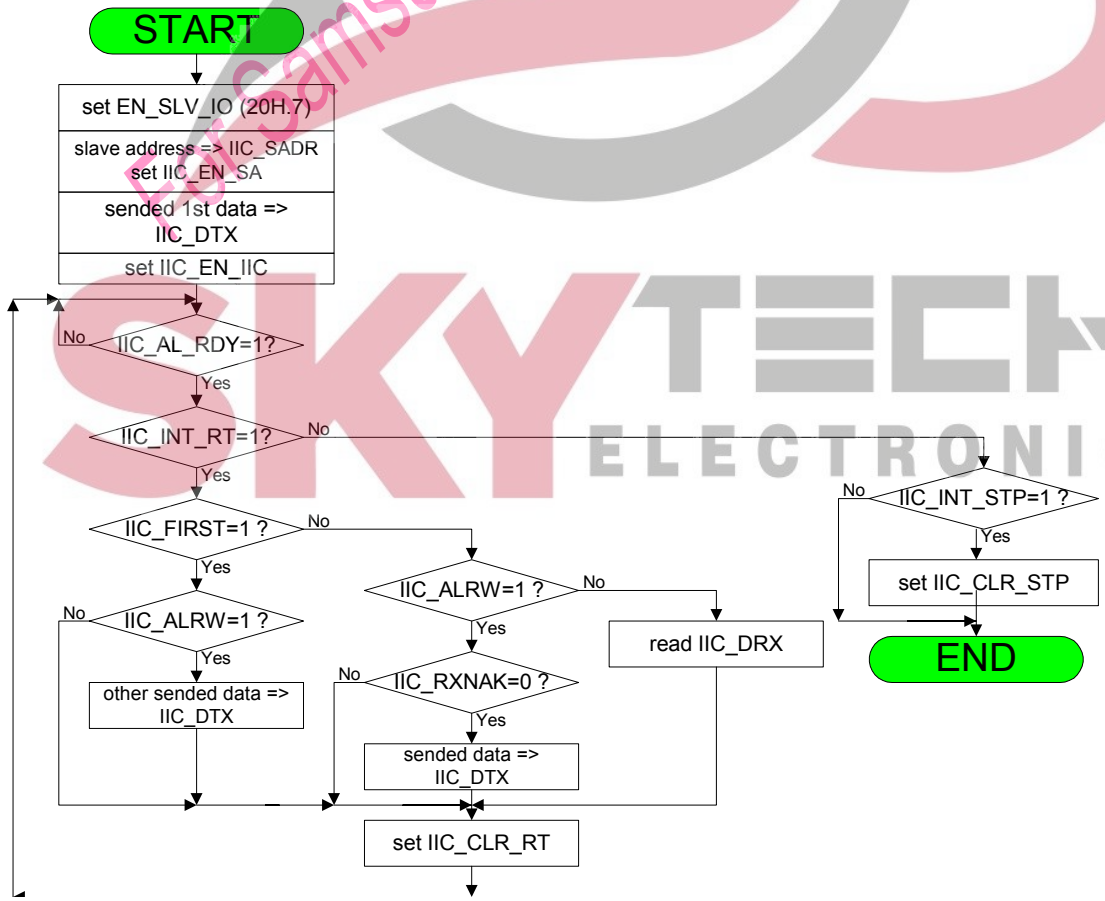
(1) IIC write mode :



(2) IIC read mode :

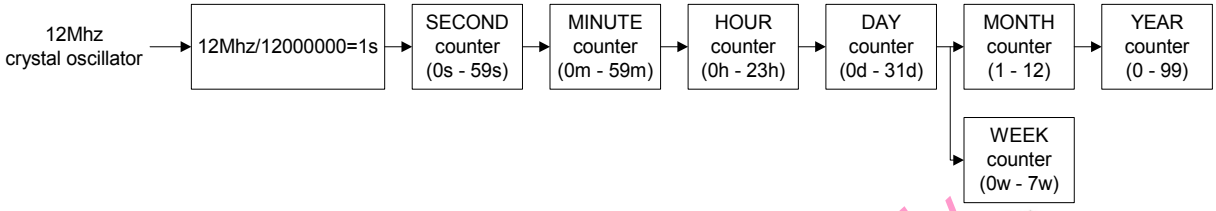


WT61P8 Slave IIC Flow Chart



4.14. RTC(Real Time Clock)

RTC Function Block:



RTC Error for 24Hours:

(a) Because WT61P8 H/W RTC function only includes counters. The counters don't have any errors.

(b) If the external 12Mhz crystal oscillator has +/- 0.01% error. For 24hours, the accumulative error is +/- (60sec x 60min x 24hr x 0.01%) = +/- 8.64sec, so system must select very accurate crystal. Otherwise, F/W must has crystal oscillator(RTC) calibration function.

RTC Alarm Polling Flag Register

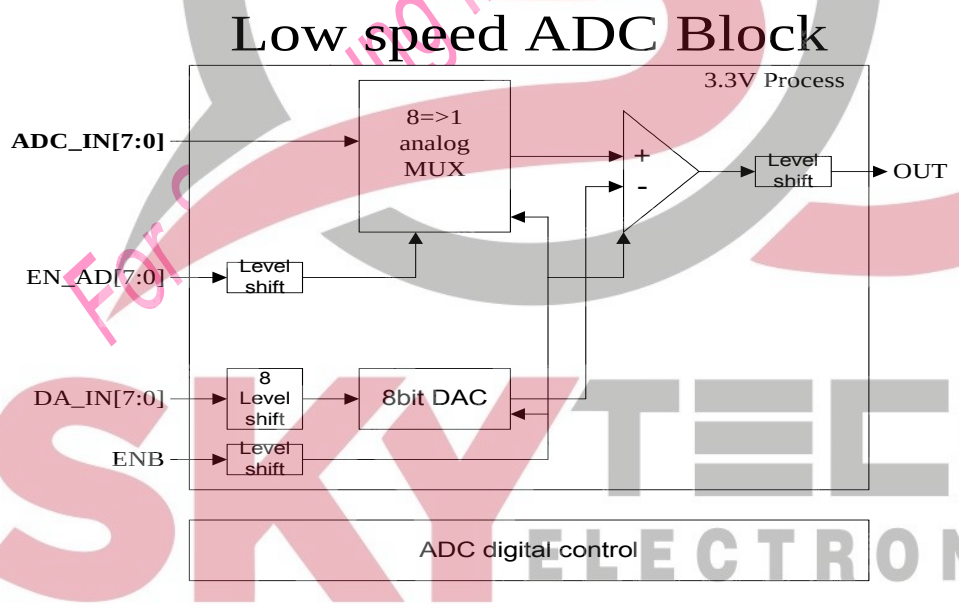
Index	Default	R/W	Bit	Name	Description
B0	00	R/W	7	EN_RTC	1: Enable RTC, when set time, need to set EN_RTC=0 0: Disable RTC,
			6-5	Reserved	
		R	4	RTC_ALARM	1: Event of alarm 0: No event of alarm
		R	3	RTC_1S	1: Event of RTC 1s 0: No event of RTC 1s
		R/W	2	ALARM_EN	1: Enable alarm 0: Disable alarm
		W	1	CLR_ALARM	1: Clear event alarm interrupt 0: No clear event alarm interrupt
		W	0	CLR_RTC_1S	1: Clear event RTC 1s interrupt 0: No clear event RTC 1s interrupt
B1	00	R/W	7	Reserved	
			6-0	RTC_SEC[6:0]	Second coded in BCD, range is 0~59. SEC [6:4] represents 10 seconds. SEC[3:0] represents seconds.
B2	00	R/W	7	Reserved	
			6-0	RTC_MIN[6:0]	Minute coded in BCD, range is 0~59. MIN[6:4] represents 10 minutes. MIN[3:0] represents minutes.
B3	00	R/W	7-6	Reserved	
			5-0	RTC_HOUR[5:0]	Hour coded in BCD, range is 0~23. HOUR[5:4] represents 10 hours. HOUR[3:0] represents hours.
B4	01	R/W	7-6	Reserved	
			5-0	RTC_DAY[5:0]	Day of month coded in BCD, range is 1~31. DAY[5:4] represents 10 days. DAY[3:0] represents days.
B5	00	R/W	7-3	Reserved	
			2-0	RTC_WEEK[2:0]	Day of week. 000 : Sunday 001 : Monday 010 : Tuesday 011 : Wednesday 100 : Thursday 101 : Friday 110 : Saturday
B6	01	R/W	7-4	Reserved	

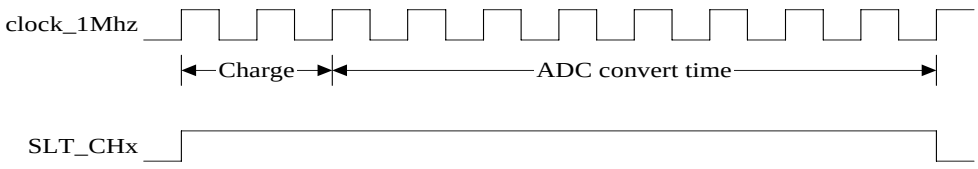
			3-0	RTC_MONTH [3:0]	Month. 0001 : January 0010 : February 0011 : March 0100 : April 0101 : May 0110 : June 0111 : July. 1000 : August 1001 : September 1010 : October 1011 : November 1100 : December
B7	00	R/W	7-0	RTC_YEAR[7:0]	Year coded in BCD, range is 0~99. YEAR[7:4] represents 10 years. YEAR [3:0] represents years.
B9	00	R/W	7	RTC_MAE	Minute alarm enable. 0 : Disable. 1 : Enable.
			6-0	RTC_AMIN[6:0]	Alarm minute coded in BCD. Range is 0 ~ 59.
BA	00	R/W	7	RTC_HAE	Hour alarm enable. 0 : Disable. 1 : Enable.
			6	Reserved	
			5-0	RTC_AHOUR [5:0]	Alarm hour coded in BCD. Range is 0 ~ 23.
BB	01	R/W	7	RTC_DAE	Day alarm enable. 0 : Disable. 1 : Enable.
			6	Reserved	
			5-0	RTC_ADAY[5:0]	Alarm day coded in BCD. Range is 1 ~ 31.
BC	00	R/W	7	RTC_WAE	Day of week alarm enable. 0 : Disable. 1 : Enable.
			6-3	Reserved	
			2-0	RTC_AWEEK [2:0]	Alarm day of week. Range is 0 ~ 6.
BD	01	R/W	7	RTC_TAE	Month alarm enable. 0 : Disable. 1 : Enable.
			6-4	Reserved	
			3-0	RTC_AMONTH [3:0]	Alarm month coded in BCD. Range is 1 ~ 12.

4.15. Low Speed ADC (for key scan)

The Analog-to-Digital Converter (ADC) is 8-bit resolution with 8 selectable input channels. When EN_AD_IO[7:0](register 23) are set, IO PAD is configured as ADC input and IO PAD pull-high resistor is disabled. When EN_AD[7:0] select which channel is converted and STR_CVT is set, it will reset the AD_DATA register and start converting. After the conversion is done, the STR_CVT bit is clear and valid data is stored in AD_DATA. The total conversion time is 10us. If program wants to make a new conversion, it writes STR_CVT register again and it will start another conversion.

Index	Default	R/W	Bit	Name	Description
D0	80	R/W	7	PD_LADC	1:Power down low speed ADC(default) 0:Enable low speed ADC
			6	STR_CVT	1:Start ADC converter 1 => 0 : convert finish
			5	ADC_BIG	1:Select wake up ADC compare bigger
			4	EN_ADC_WK	1:Enable ADC wake up mode 0:Disable ADC wake up mode
			3-0	Reserved	
D1	00	R	7-0	AD_DATA[7:0]	ADC convert data
D2	80	R/W	7-0	ADC_WK_V[7:0]	ADC wake up compare voltage
D3	00	R/W	7-0	EN_AD[7:0]	1:Enable ADC IO of CH[x] 0:Disable Enable ADC IO of CH[x]

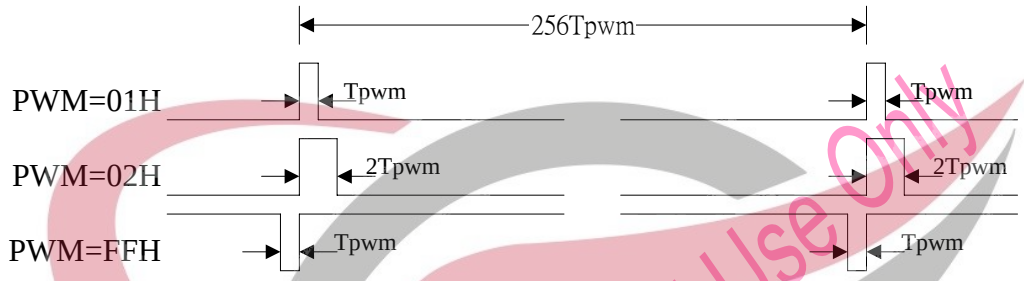




4.16. PWM

PWM0 ~ PWM7 : 8-bit PWM and 3.3V push-pull output, shared with I/O GPIO E and GPIO A.
LPWM0 : 8-bit low frequency PWM shared with GPIO E4.

The corresponding PWM register controls the PWM duty cycle. Duty cycle range is from 0/256 to 255/256.



If PWM_CLK register = 0 , Tpwm=1/12Mhz(at MCU clock=12MHz)=84ns
If PWM_CLK register = 1 , Tpwm=1/1Mhz=1us

LPWM output clock=1Mhz / ((PWMLCx +1)* 256) = **256us * (PWMLCx+1)**
When PWMLC=24, LPWM output clock=6.400ms=156.25hz
When PWMLC=25, LPWM output clock=6.656ms=150.24hz
When PWMLC=26, LPWM output clock=6.912ms=144.68hz

Index	Default	R/W	Bit	Name	Description
F0	80	R/W	7-0	PWM0[7:0]	Select duty cycle of PWM0 output. 00000000: duty cycle = 0 00000001: duty cycle = 1/256 00000010: duty cycle = 2/256 : 11111110: duty cycle = 254/256 11111111: duty cycle = 255/256
F1	80	R/W	7-0	PWM1[7:0]	Select duty cycle of PWM1 output.
F2	80	R/W	7-0	PWM2[7:0]	Select duty cycle of PWM2 output.
F3	80	R/W	7-0	PWM3[7:0]	Select duty cycle of PWM3 output.
F4	80	R/W	7-0	PWM4[7:0]	Select duty cycle of PWM4 output.
F5	80	R/W	7-0	PWM5[7:0]	Select duty cycle of PWM5 output.
F6	80	R/W	7-0	PWM6[7:0]	Select duty cycle of PWM6 output.
F7	80	R/W	7-0	PWM7[7:0]	Select duty cycle of PWM7 output.
F8	00	R/W	7	Reserved	
			6-0	PWM_CLK[6:0]	Select LPWM clock
F9	00	R/W	7-0	PWML[7:0]	LPWM output data

5. ALL Register Map

Index	Default	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
01	80	R/W	RST_NDF	OSC_OFF	MCU_OFF	PWM_CLK		XTAL_CLK	CHG_CLK[1]	CHG_CLK[0]
02	00	R/W	CEC_WAKE	IR_WAKE	ADC_WAKE	SI2C_WAKE	DDC_WAKE[1]	DDC_WAKE[0]	HV_WAKE[1]	HV_WAKE[0]
03	00	R/W	RTC_1S_WAKE	ALARM_WAKE	UART_WAKE [1]	UART_WAKE [0]	IRQ_WAKE[3]	IRQ_WAKE[2]	IRQ_WAKE[1]	IRQ_WAKE[0]
04	00	R	CEC_TOG	IR_ TOG	ADC_ TOG	SI2C_TOG	DDC_ TOG[1]	DDC_ TOG[0]	HV_ TOG[1]	HV_ TOG[0]
05	00	R	RTC_1S_TOG	ALARM_TOG	UART_TOG[1]	UART_TOG[0]	IRQ_ TOG[3]	IRQ_ TOG[2]	IRQ_ TOG[1]	IRQ_ TOG[0]
06	00	W	CLR_IN_TOG							
08	00	W	DIS_WDT						WDT[1]	WDT[0]
10	00	R/W			GPIOA_OE[5]	GPIOA_OE[4]	GPIOA_OE[3]	GPIOA_OE[2]	GPIOA_OE[1]	GPIOA_OE[0]
11	00	R/W		GPIOB_OE[6]	GPIOB_OE[5]	GPIOB_OE[4]	GPIOB_OE[3]	GPIOB_OE[2]	GPIOB_OE[1]	GPIOB_OE[0]
12	00	R/W	GPIOC_OE[7]	GPIOC_OE[6]	GPIOC_OE[5]	GPIOC_OE[4]	GPIOC_OE[3]	GPIOC_OE[2]	GPIOC_OE[1]	GPIOC_OE[0]
13	00	R/W	GPIOD_OE[7]	GPIOD_OE[6]	GPIOD_OE[5]	GPIOD_OE[4]	GPIOD_OE[3]	GPIOD_OE[2]	GPIOD_OE[1]	GPIOD_OE[0]
14	00	R/W	GPIOE_OE[7]	GPIOE_OE[6]	GPIOE_OE[5]	GPIOE_OE[4]	GPIOE_OE[3]	GPIOE_OE[2]	GPIOE_OE[1]	GPIOE_OE[0]
15	00	R/W			GPIOA_D[5]	GPIOA_D[4]	GPIOA_D[3]	GPIOA_D[2]	GPIOA_D[1]	GPIOA_D[0]
16	00	R/W		GPIOB_D[6]	GPIOB_D[5]	GPIOB_D[4]	GPIOB_D[3]	GPIOB_D[2]	GPIOB_D[1]	GPIOB_D[0]
17	00	R/W	GPIOC_D[7]	GPIOC_D[6]	GPIOC_D[5]	GPIOC_D[4]	GPIOC_D[3]	GPIOC_D[2]	GPIOC_D[1]	GPIOC_D[0]
18	00	R/W	GPIOD_D[7]	GPIOD_D[6]	GPIOD_D[5]	GPIOD_D[4]	GPIOD_D[3]	GPIOD_D[2]	GPIOD_D[1]	GPIOD_D[0]
19	00	R/W	GPIOE_D[7]	GPIOE_D[6]	GPIOE_D[5]	GPIOE_D[4]	GPIOE_D[3]	GPIOE_D[2]	GPIOE_D[1]	GPIOE_D[0]
1A	00	R/W			GPIOA_PHN[5]	GPIOA_PHN[4]	GPIOA_PHN[3]	GPIOA_PHN[2]	GPIOA_PHN[1]	GPIOA_PHN[0]
1B	00	R/W		GPIOB_PHN[6]	GPIOB_PHN[5]	GPIOB_PHN[4]	GPIOB_PHN[3]	GPIOB_PHN[2]	GPIOB_PHN[1]	GPIOB_PHN[0]
1C	00	R/W	GPIOC_PHN[7]	GPIOC_PHN[6]	GPIOC_PHN[5]	GPIOC_PHN[4]	GPIOC_PHN[3]	GPIOC_PHN[2]	GPIOC_PHN[1]	GPIOC_PHN[0]
1D	00	R/W	GPIOD_PHN[7]	GPIOD_PHN[6]	GPIOD_PHN[5]	GPIOD_PHN[4]	GPIOD_PHN[3]	GPIOD_PHN[2]	GPIOD_PHN[1]	GPIOD_PHN[0]
1E	00	R/W	GPIOE_PHN[7]	GPIOE_PHN[6]	GPIOE_PHN[5]	GPIOE_PHN[4]	GPIOE_PHN[3]	GPIOE_PHN[2]	GPIOE_PHN[1]	GPIOE_PHN[0]
20	00	R/W	EN_SLV_IO	EN_UART0_IO	EN_UART1_IO	EN_CEC_IO	EN_2DDC_IO	EN_LPWM_IO	--	--
21	00	R/W	EN_P0_IO[7]	EN_P0_IO[6]	EN_P0_IO[5]	EN_P0_IO[4]	EN_P0_IO[3]	EN_P0_IO[2]	EN_P0_IO[1]	EN_P0_IO[0]
22	00	R/W	EN_P1_IO[7]	EN_P1_IO[6]	EN_P1_IO[5]	EN_P1_IO[4]	EN_P1_IO[3]	EN_P1_IO[2]	EN_P1_IO[1]	EN_P1_IO[0]
23	00	R/W	EN_AD_IO[7]	EN_AD_IO[6]	EN_AD_IO[5]	EN_AD_IO[4]	EN_AD_IO[3]	EN_AD_IO[2]	EN_AD_IO[1]	EN_AD_IO[0]
24	00	R/W	EN_PWM_IO[7]	EN_PWM_IO[6]	EN_PWM_IO[5]	EN_PWM_IO[4]	EN_PWM_IO[3]	EN_PWM_IO[2]	EN_PWM_IO[1]	EN_PWM_IO[0]
30	00	R/W	IE1_1DDC	IE1_2DDC	IE1_HV1	IE1_HV2	IE1_IR	IE1_KADC	IE1_RTC_1S	IE1_ALARM
31	00	R/W				IE1_CEC	IE1_IRQ[3]	IE1_IRQ[2]	IE1_IRQ[1]	IE1_IRQ[0]
32	00	R/W	IE2_1DDC	IE2_2DDC	IE2_HV1	IE2_HV2	IE2_IR	IE2_KADC	IE2_RTC_1S	IE2_ALARM
33	00	R/W				IE2_CEC	IE2_IRQ[3]	IE2_IRQ[2]	IE2_IRQ[1]	IE2_IRQ[0]
34	00	R	IF1_1DDC	IF1_2DDC	IF1_HV1	IF1_HV2	IF1_IR	IF1_KADC	IF1_RTC_1S	IF1_ALARM
35	00	R				IF1_CEC	IF1_IRQ[3]	IF1_IRQ[2]	IF1_IRQ[1]	IF1_IRQ[0]
36	00	R	IF2_1DDC	IF2_2DDC	IF2_HV1	IF2_HV2	IF2_IR	IF2_KADC	IF2_RTC_1S	IF2_ALARM
37	00	R				IF2_CEC	IF2_IRQ[3]	IF2_IRQ[2]	IF2_IRQ[1]	IF2_IRQ[0]
3A	00	R/W	EVT_IRQ[3]	EVT_IRQ[2]	EVT_IRQ[1]	EVT_IRQ[0]	CLR_IRQ[3]	CLR_IRQ[2]	CLR_IRQ[1]	CLR_IRQ[0]
3B	00	R/W	IRQ_CHG[3]	IRQ_CHG[2]	IRQ_CHG[1]	IRQ_CHG[0]	IRQ_EDGE[3]	IRQ_EDGE[2]	IRQ_EDGE[1]	IRQ_EDGE[0]
40	00	R/W	EN_HV1_CNT	EN_VIN1_INT	EN_H16M1_INT	EN_V1OV_INT	EN_H1OV_INT			
41	00	R	HV1_INT	VIN1_INT	HIN1_INT	V1_OVRFL	H1_OVRFL			
42	00	R/W	CLR_VIN1_INT	CLR_HIN1_INT	CLR_V1OV_INT	CLR_H1OV_INT	HV1_COMP	EN_HV1_COMP	H1_LWP[1]	H1_LWP[0]
43	00	R					HF1[3]	HF1[2]	HF1[1]	HF1[0]
44	00	R	HF1[11]	HF1[10]	HF1[9]	HF1[8]	HF1[7]	HF1[6]	HF1[5]	HF1[4]
45	00	R/W	H1_LOV[7]	H1_LOV[6]	H1_LOV[5]	H1_LOV[4]	H1_LOV[3]	H1_LOV[2]	H1_LOV[1]	H1_LOV[0]
46	00	R			VF1[5]	VF1[4]	VF1[3]	VF1[2]	VF1[1]	VF1[0]
47	00	R	VF1[13]	VF1[12]	VF1[11]	VF1[10]	VF1[9]	VF1[8]	VF1[7]	VF1[6]
48	00	R/W	V1_LOV[7]	V1_LOV[6]	V1_LOV[5]	V1_LOV[4]	V1_LOV[3]	V1_LOV[2]	V1_LOV[1]	V1_LOV[0]
50	00	R/W	EN_HV2_CNT	EN_VIN2_INT	EN_H16M2_INT	EN_V2OV_INT	EN_H2OV_INT			
51	00	R	HV2_INT	VIN2_INT	HIN2_INT	V2_OVRFL	H2_OVRFL			
52	00	R/W	CLR_VIN2_INT	CLR_HIN2_INT	CLR_V2OV_INT	CLR_H2OV_INT	HV2_COMP	EN_HV2_COMP	H2_LWP[1]	H2_LWP[0]
53	00	R					HF2[3]	HF2[2]	HF2[1]	HF2[0]
54	00	R	HF2[11]	HF2[10]	HF2[9]	HF2[8]	HF2[7]	HF2[6]	HF2[5]	HF2[4]
55	00	R/W	H2_LOV[7]	H2_LOV[6]	H2_LOV[5]	H2_LOV[4]	H2_LOV[3]	H2_LOV[2]	H2_LOV[1]	H2_LOV[0]
56	00	R			VF2[5]	VF2[4]	VF2[3]	VF2[2]	VF2[1]	VF2[0]
57	00	R	VF2[13]	VF2[12]	VF2[11]	VF2[10]	VF2[9]	VF2[8]	VF2[7]	VF2[6]
58	00	R/W	V2_LOV[7]	V2_LOV[6]	V2_LOV[5]	V2_LOV[4]	V2_LOV[3]	V2_LOV[2]	V2_LOV[1]	V2_LOV[0]
60	00	R/W	EN_IR	IR_SEDG	IR_RF	EN_OV_INT	PRE_SCAL[1]	PRE_SCAL[0]	CLR_IR_INT	
61	04	R						IR_HL	IR_OVFLW	IR_INT
62	00	R	IR_CNT[7]	IR_CNT[6]	IR_CNT[5]	IR_CNT[4]	IR_CNT[3]	IR_CNT[2]	IR_CNT[1]	IR_CNT[0]
70	00	R/W	EN_CEC			CEC_BUSY		CEC_L_3600US		
71	20	R/W	CEC_TR	CEC_O_EOM	CEC_RXACK					
72	00	R/W	CEC_I_STR	CEC_I_EOM	CEC_TXACK	CEC_NACK_INT				
73	00	R	CEC_INT	CEC_TX_INT	CEC_RX_INT	CEC_DLOSS	CEC_TM_OUT	CEC_LINE _ERROR		
74	00	R/W		CLR_TX_INT	CLR_RX_INT	CLR_DLOSS	CLR_ TM_OUT	CLR_ LINE_ERROR		
75	FF	R/W	CEC_DTX[7]	CEC_DTX[6]	CEC_DTX[5]	CEC_DTX[4]	CEC_DTX[3]	CEC_DTX[2]	CEC_DTX[1	CEC_DTX[0]
76	00	R	CEC_DRX[7]	CEC_DRX[6]	CEC_DRX[5]	CEC_DRX[4]	CEC_DRX[3]	CEC_DRX[2]	CEC_DRX[1]	CEC_DRX[0]
80	00	R/W	VDC_EN_DDC	VDC_CLR_RT	VDC_CLR_STP	VDC_WAIT	VDC_ENADR8			VDC_TXNAK
81	00	R	VDC_AL_RDY	VDC_INT_RT	VDC_INT_STOP			VDC_FIRST	VDC_ALRW	VDC_RXNAK
82	00	R						VDC_BB	VDC_SLV2	VDC_SLV1
83	FF	R/W	VDC_DTX1[7]	VDC_DTX1[6]	VDC_DTX1[5]	VDC_DTX1[4]	VDC_DTX1[3]	VDC_DTX1[2]	VDC_DTX1[1]	VDC_DTX1[0]
84	FF	R/W	VDC_DTX2[7]	VDC_DTX2[6]	VDC_DTX2[5]	VDC_DTX2[4]	VDC_DTX2[3]	VDC_DTX2[2]	VDC_DTX2[1]	VDC_DTX2[0]
85	00	R	VDC_DRX[7]	VDC_DRX[6]	VDC_DRX[5]	VDC_DRX[4]	VDC_DRX[3]	VDC_DRX[2]	VDC_DRX[1]	VDC_DRX[0]

86	00	R/W	VDC_SADR1[6]	VDC_SADR1[5]	VDC_SADR1[4]	VDC_SADR1[3]	VDC_SADR1[2]	VDC_SADR1[1]	VDC_SADR1[0]	VDC_EN_SA1
87	00	R/W	VDC_SDAR2[6]	VDC_SDAR2[5]	VDC_SDAR2[4]	VDC_SDAR2[3]	VDC_SDAR2[2]	VDC_SDAR2[1]	VDC_SDAR2[0]	VDC_EN_SA2
90	00	R/W	DVC_EN_DDC	DVC_CLR_RT	DVC_CLR_STP	DVC_WAIT	DVC_ENADR8			DVC_TXNAK
91	00	R	DVC_AL_RDY	DVC_INT_RT	DVC_INT_STOP			DVC_FIRST	DVC_ALRW	DVC_RXNAK
92	00	R						DVC_BB	DVC_SLV2	DVC_SLV1
93	FF	R/W	DVC_DTX1[7]	DVC_DTX1[6]	DVC_DTX1[5]	DVC_DTX1[4]	DVC_DTX1[3]	DVC_DTX1[2]	DVC_DTX1[1]	DVC_DTX1[0]
94	FF	R/W	DVC_DTX2[7]	DVC_DTX2[6]	DVC_DTX2[5]	DVC_DTX2[4]	DVC_DTX2[3]	DVC_DTX2[2]	DVC_DTX2[1]	DVC_DTX2[0]
95	00	R	DVC_DRX[7]	DVC_DRX[6]	DVC_DRX[5]	DVC_DRX[4]	DVC_DRX[3]	DVC_DRX[2]	DVC_DRX[1]	DVC_DRX[0]
96	00	R/W	DVC_SADR1[6]	DVC_SADR1[5]	DVC_SADR1[4]	DVC_SADR1[3]	DVC_SADR1[2]	DVC_SADR1[1]	DVC_SADR1[0]	DVC_EN_SA1
97	00	R/W	DVC_SDAR2[6]	DVC_SDAR2[5]	DVC_SDAR2[4]	DVC_SDAR2[3]	DVC_SDAR2[2]	DVC_SDAR2[1]	DVC_SDAR2[0]	DVC_EN_SA2
A0	00	R/W	IIC_EN_DDC	IIC_CLR_RT	IIC_CLR_STP	IIC_WAIT				IIC_TXNAK
A1	00	R	IIC_AL_RDY	IIC_INT_RT	IIC_INT_STOP			IIC_FIRST	IIC_ALRW	IIC_RXNAK
A2	FF	R/W	IIC_DTX1[7]	IIC_DTX1[6]	IIC_DTX1[5]	IIC_DTX1[4]	IIC_DTX1[3]	IIC_DTX1[2]	IIC_DTX1[1]	IIC_DTX1[0]
A3	00	R	IIC_DRX[7]	IIC_DRX[6]	IIC_DRX[5]	IIC_DRX[4]	IIC_DRX[3]	IIC_DRX[2]	IIC_DRX[1]	IIC_DRX[0]
A4	00	R/W	IIC_SADR1[6]	IIC_SADR1[5]	IIC_SADR1[4]	IIC_SADR1[3]	IIC_SADR1[2]	IIC_SADR1[1]	IIC_SADR1[0]	IIC_EN_SA1
B0	00	R/W	EN_RTC			RTC_ALARM	RTC_1S	ALARM_EN	CLR_ALARM	CLR_RTC_1S
B1	00	R/W		RTC_SEC[6]	RTC_SEC[5]	RTC_SEC[4]	RTC_SEC[3]	RTC_SEC[2]	RTC_SEC[1]	RTC_SEC[0]
B2	00	R/W		RTC_MIN[6]	RTC_MIN[5]	RTC_MIN[4]	RTC_MIN[3]	RTC_MIN[2]	RTC_MIN[1]	RTC_MIN[0]
B3	00	R/W			RTC_HOUR[5]	RTC_HOUR[4]	RTC_HOUR[3]	RTC_HOUR[2]	RTC_HOUR[1]	RTC_HOUR[0]
B4	01	R/W			RTC_DAY[5]	RTC_DAY[4]	RTC_DAY[3]	RTC_DAY[2]	RTC_DAY[1]	RTC_DAY[0]
B5	00	R/W						RTC_WEEK[2]	RTC_WEEK[1]	RTC_WEEK[0]
B6	01	R/W					RTC_MONTH[3]	RTC_MONTH[2]	RTC_MONTH[1]	RTC_MONTH[0]
B7	00	R/W	RTC_YEAR[7]	RTC_YEAR[6]	RTC_YEAR[5]	RTC_YEAR[4]	RTC_YEAR[3]	RTC_YEAR[2]	RTC_YEAR[1]	RTC_YEAR[0]
B8	00	R/W	RTC_SAE	RTC_ASEC[6]	RTC_ASEC[5]	RTC_ASEC[4]	RTC_ASEC[3]	RTC_ASEC[2]	RTC_ASEC[1]	RTC_ASEC[0]
B9	00	R/W	RTC_MAE	RTC_AMIN[6]	RTC_AMIN[5]	RTC_AMIN4]	RTC_AMIN[3]	RTC_AMIN[2]	RTC_AMIN[1]	RTC_AMIN[0]
BA	00	R/W	RTC_HAE		RTC_AHR[5]	RTC_AHR[4]	RTC_AHR[3]	RTC_AHR[2]	RTC_AHR[1]	RTC_AHR[0]
BB	00	R/W	RTC_DAE		RTC_ADAY[5]	RTC_ADAY[4]	RTC_ADAY[3]	RTC_ADAY[2]	RTC_ADAY[1]	RTC_ADAY[0]
BC	00	R/W	RTC_WAE					RTC_AWEEK[2]	RTC_AWEEK[1]	RTC_AWEEK[0]
BD	00	R/W	RTC_TAE				RTC_AMONTH[3]	RTC_AMONTH[2]	RTC_AMONTH[1]	RTC_AMONTH[0]
D0	80	R/W	PD_LADC	STR_CVT	ADC_BIG	EN_ADC_WK				
D1	00	R	AD_DATA[7]	AD_ DATA[6]	AD_ DATA[5]	AD_ DATA[4]	AD_ DATA[3]	AD_DATA[2]	AD_ DATA[1]	AD_ DATA[0]
D2	80	R/W	ADC_WK_V[7]	ADC_WK_V[6]	ADC_WK_V[5]	ADC_WK_V[4]	ADC_WK_V[3]	ADC_WK_V[2]	ADC_WK_V[1]	ADC_WK_V[0]
D3	80	R/W	EN_AD[7]	EN_AD[6]	EN_AD[5]	EN_AD[4]	EN_AD[3]	EN_AD[2]	EN_AD[1]	EN_AD[0]
F0	80	R/W	PWM0[7]	PWM0[6]	PWM0[5]	PWM0[4]	PWM0[3]	PWM0[2]	PWM0[1]	PWM0[0]
F1	80	R/W	PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[2]	PWM1[0]
F2	80	R/W	PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]
F3	80	R/W	PWM3[7]	PWM3[6]	PWM3[5]	PWM3[4]	PWM3[3]	PWM3[2]	PWM3[2]	PWM3[0]
F4	80	R/W	PWM4[7]	PWM4[6]	PWM4[5]	PWM4[4]	PWM4[3]	PWM4[2]	PWM4[1]	PWM4[0]
F5	80	R/W	PWM5[7]	PWM5[6]	PWM5[5]	PWM5[4]	PWM5[3]	PWM5[2]	PWM5[2]	PWM5[0]
F6	80	R/W	PWM6[7]	PWM6[6]	PWM6[5]	PWM6[4]	PWM6[3]	PWM6[2]	PWM6[1]	PWM6[0]
F7	80	R/W	PWM7[7]	PWM7[6]	PWM7[5]	PWM7[4]	PWM7[3]	PWM7[2]	PWM7[2]	PWM7[0]
F8	00	R/W		PWM_CLK[6]	PWM_CLK[5]	PWM_CLK[4]	PWM_CLK[3]	PWM_CLK[2]	PWM_CLK[1]	PWM_CLK[0]
F9	00	R/W	PWML[7]	PWML[6]	PWML[5]	PWML[4]	PWML[3]	PWML[2]	PWML[1]	PWML[0]

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Parameter	Min.	Max.	Units
DC Supply Voltage (VDD)	-0.3	3.6	V
Storage temperature	-25	125	°C
Operating temperature	-10	85	°C

***Note: Stresses above those listed may cause permanent damage to the devices**

6.2. Power Supply (VDD=3.3v) at crystal oscillator = 12MHz

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{VDD12M}	Normal operation current at 12Mhz operating	No load on output		12		mA
I_{VDD6M}	Normal operation current at 6Mhz operating	No load on output		8		mA
I_{VDD3M}	Normal operation current at 3Mhz operating	No load on output		6.5		mA
I_{VDD1M}	Normal operation current at 1Mhz operating	No load on output		5		mA
$I_{VDDhold}$	RTC operation current (MCU is hold)	No load on output		2		mA
I_{VDDS}	Standby current	No load on output		100		uA

6.3. Power Supply (VDD=3.3v) at crystal oscillator = 24MHz

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{VDD24M}	Normal operation current at 24Mhz operating	No load on output		20		mA
I_{VDD12M}	Normal operation current at 12Mhz operating	No load on output		13		mA
I_{VDD6M}	Normal operation current at 6Mhz operating	No load on output		9.5		mA
I_{VDD2M}	Normal operation current at 2Mhz operating	No load on output		7		mA
$I_{VDDhold}$	RTC operation current (MCU is hold)	No load on output		3		mA
I_{VDDS}	Standby current	No load on output		100		uA

6.4. Digital I/O

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{T+}	Schmitt trigger Low-to-High threshold		2.1		5.5	V

	point					
V_{T-}	Schmitt trigger High-to-Low threshold point				1	V
V_{OH}	Output high voltage	I_{OH} = 4mA	2.4			V
V_{OL}	Output low voltage(Note 1)	I_{OL} = 4mA			0.4	V
V_{OH}	Output high voltage(GPIOE0~GPIOE3)	I_{OH} = 8mA	2.4			V
V_{OL}	Output low voltage(GPIOE0~GPIOE3)	I_{OL} = 8mA			0.4	V
I_{OZ}	Tri-state leakage current	V_O = 0 or 3.3V		±0.01	±1	μA
R_{PD}	Pull up resistor			60		KΩ

Note 1: Including GPIOA0~GPIOA5, DSAL1, DSCL1, GPIOB0~GPIOB6, GPIOC0~GPIOC7, GPIOD0~GPIOD7, GPIOE4~GPIOE7

Note 2: GPIOC3,GPIOC2,GPIOC1,GPIOC0,GPIOD2,GPIOD3,GPIOD4,GPIOD5 MAX input are +3.6v (=3.3v+0.3v) and the other GPIOs MAX input is +5.5v (=5.0v+0.5v)

6.5. ADC Converter

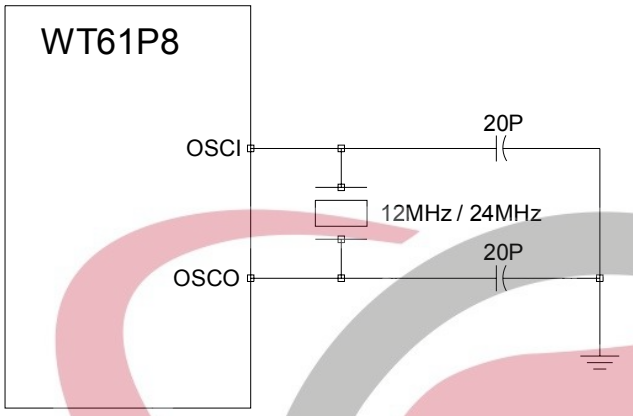
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AN}	Analog input voltage range		V_{SS}		V_{DD}	V

6.6. Low VDD Reset

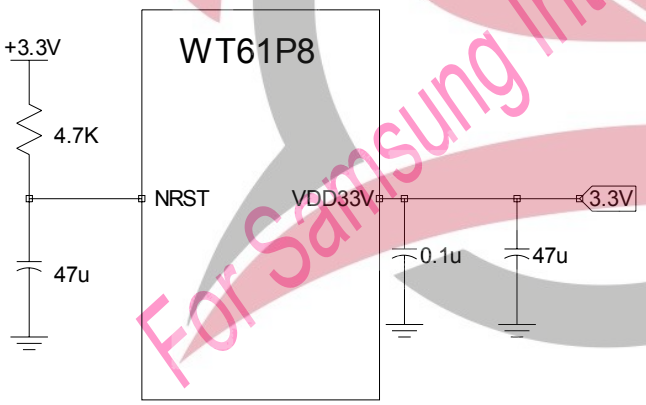
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{LVD}	Low VDD Reset Voltage			2.7		V

7. Typical application circuit

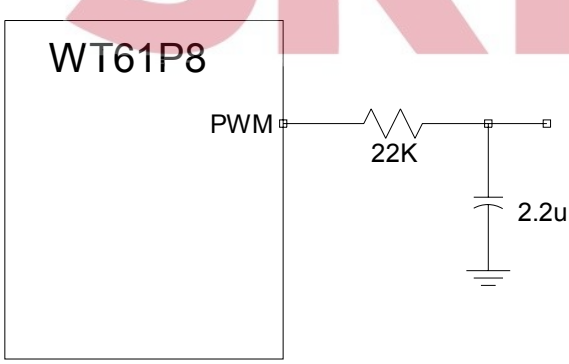
7.1. Crystal Oscillator



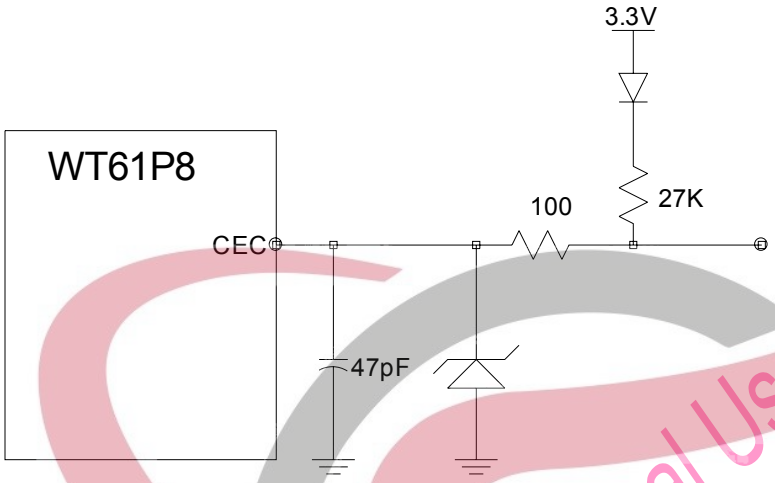
7.2. NRST Pin and VDD Pin



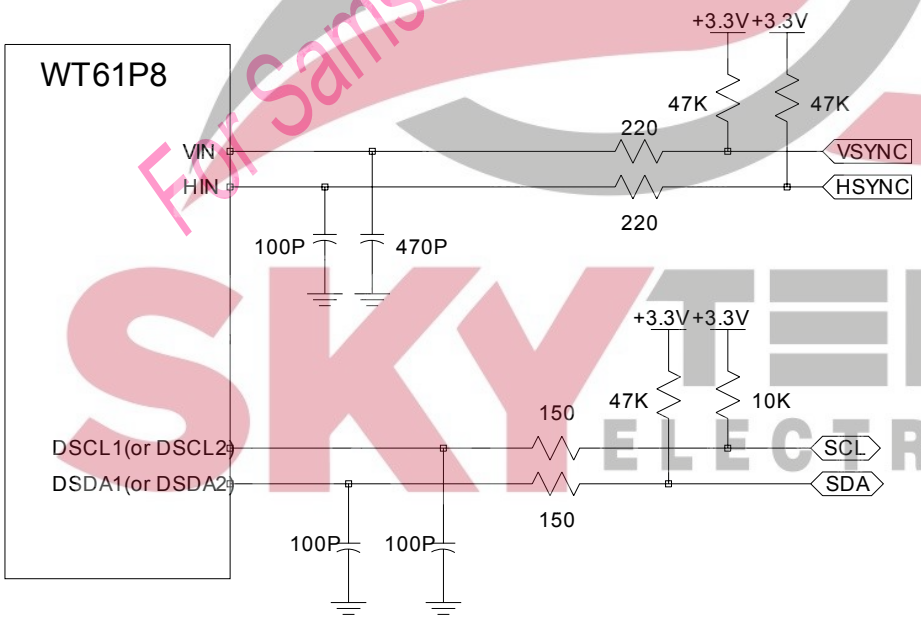
7.3. PWM Output



7.4. CEC

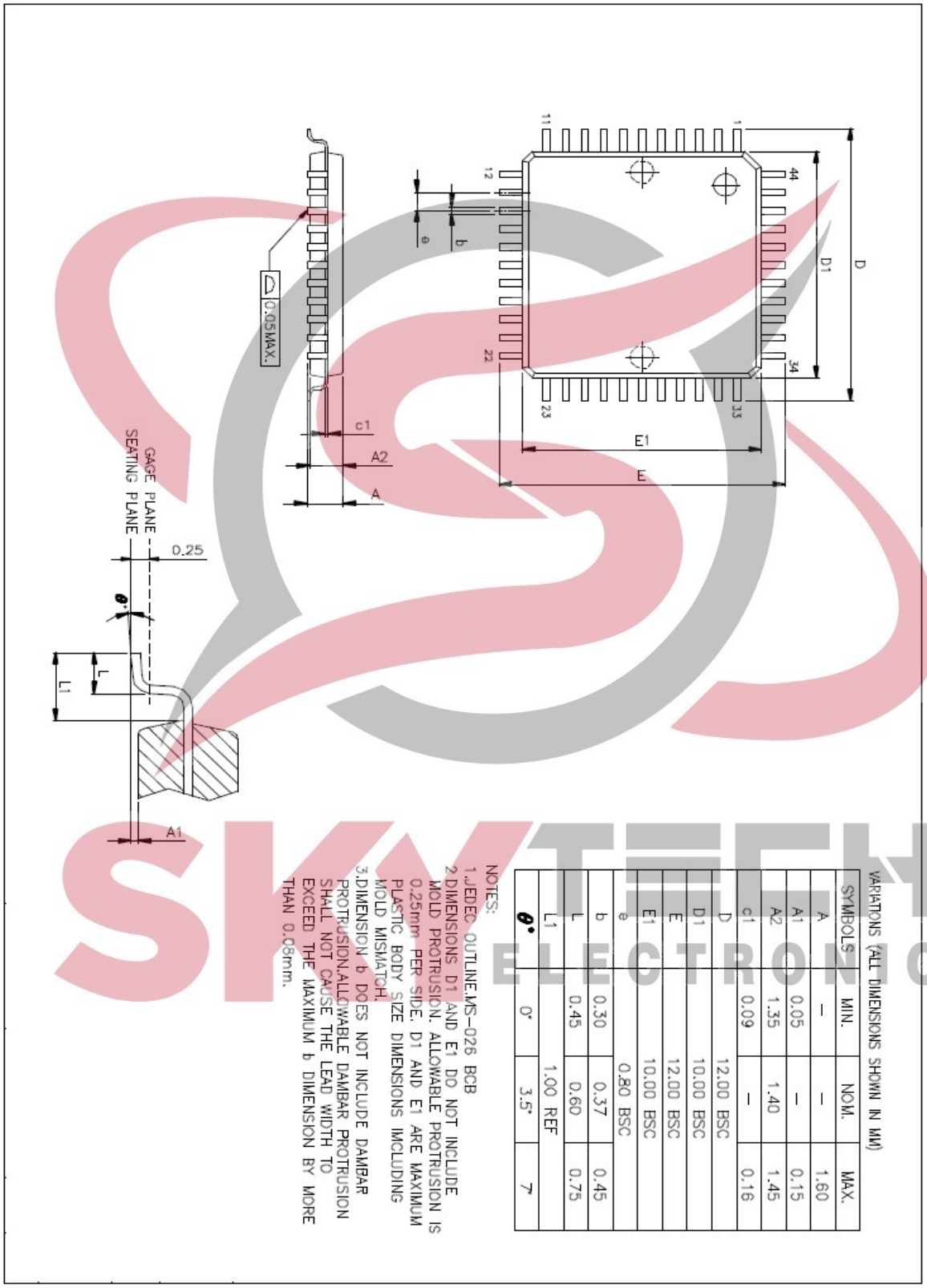


7.5. Hsync,Vsync and IIC Interface Protection



8. Package Dimension

8.1. 44pin LQFP

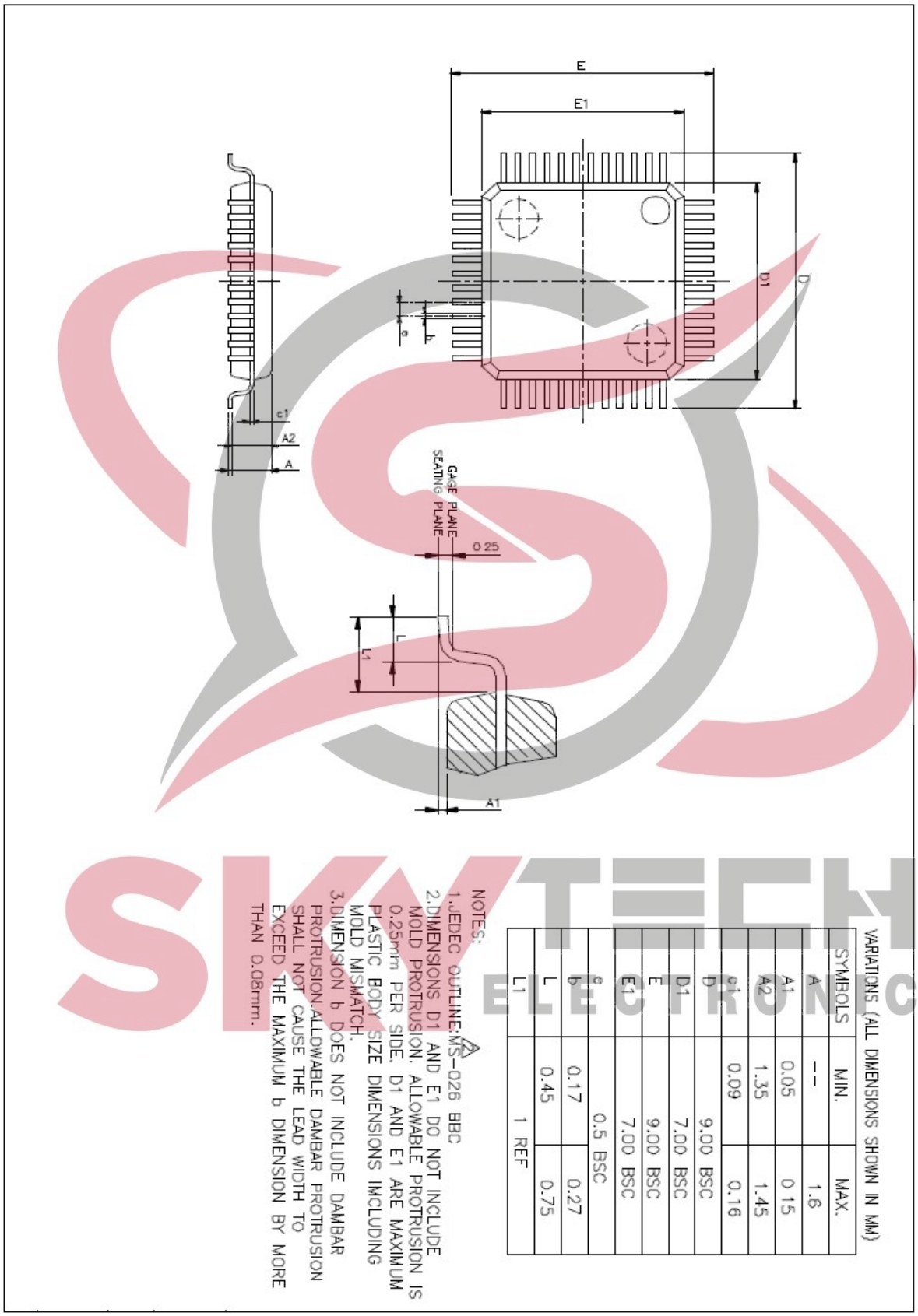


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
c1	0.09	—	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1		1.00 REF	
θ°	0°	3.5°	7°

NOTES:
1.JEDEC OUTLINE:MS-026 BCB
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

8.2. 48pin LQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

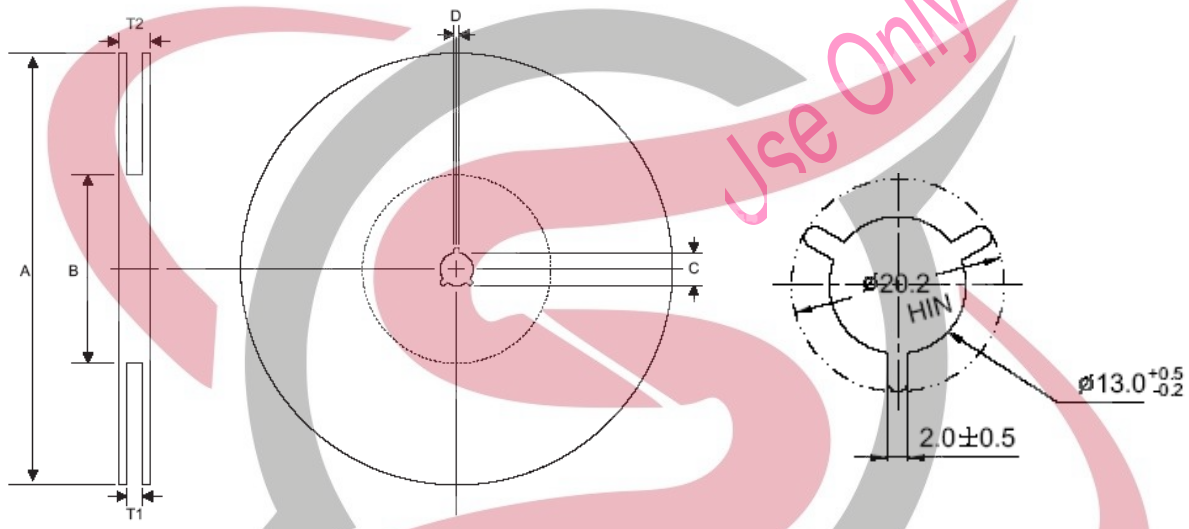
SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

8.3. Product Tray and Tape & Reel specifications

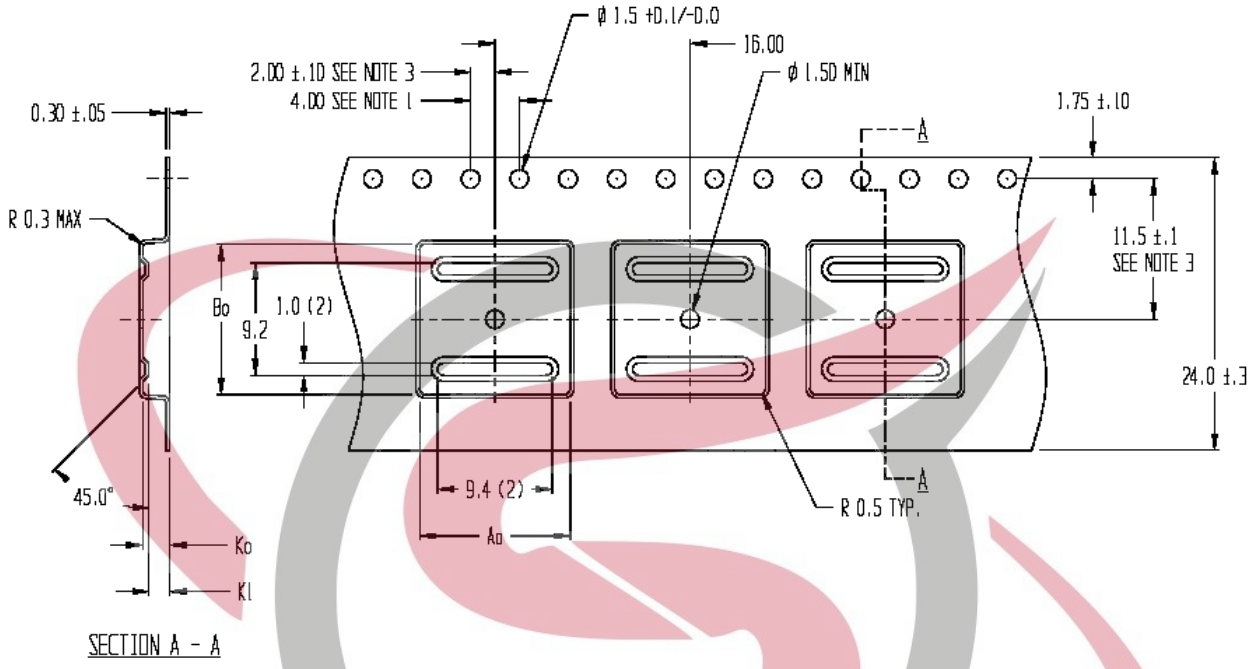
Package Type	EA/TRAY	TRAY/BOX	EA/BOX	Tapping (EA/Reel)
LQFP 44pin (10x10mm)	160	10	1600	1500

8.3.1. Reel Dimensions



Symbol	Description	Dimensions in mm	
A	Reel Outer Diameter	330	
B	Reel Inner Diameter	100	
C	Spindle Hole Diameter	13 + 0.5 - 0.2	
D	Key Slit Width	2.0 ± 0.5	
T1	Space Between Flange	LQFP 44L (10x10mm)	24.8 + 0.6 - 0.4
T2	Reel Thickness	LQFP 44L (10x10mm)	30.2

8.3.2. LQFP44L Carrier Tape Dimensions



Symbol	Description	Dimensions in mm
Ao	Cavity Length	12.35
Bo	Cavity width	12.35
Ko	Cavity Depth	2.20
K1	Cavity Depth	1.70

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.